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Commercial off the shelf direct digital synthesizers for digital array radar

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THESIS

COMMERCIAL OFF THE SHELF DIRECT DIGITAL SYNTHESIZERS FOR DIGITAL ARRAY RADAR

by

Winston Ong

December 2005

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Up until the 1980s, conventional radar systems consisted primarily of analog circuits, which are costly to build and compatible only to a narrow band of operations. Modern digital technology offers increasing capabilities at a lower cost making it attractive for modern radar application. The Direct Digital Synthesizer (DDS) is one such example of digital technology that is now routinely found in newer radar system designs. The DDS characteristics that most attract radar-system designers are precision frequency tuning, phase offset control, and linear "chirp" capability.

This study discusses the option of incorporating DDS for use in a digital pulsed and/or frequency modulated continuous wave (FMCW) radar, and examined the necessary adaptations such as up-converting baseband signals from DDS to a radar transmission frequency, viable transmit and receive waveforms and the synchronization problem relating to synchronizing the many radiating elements that could range from a few to possibly thousands.

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COMMERCIAL OFF THE SHELF DIRECT DIGITAL SYNTHESIZERS FOR DIGITAL ARRAY RADAR

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ABSTRACT

Up until the 1980s, conventional radar systems consisted primarily of analog circuits, which are costly to build and compatible only to a narrow band of operations. Modern digital technology offers increasing capabilities at a lower cost making it attractive for modern radar application. The Direct Digital Synthesizer (DDS) is one such example of digital technology that is now routinely found in newer radar system designs. The DDS characteristics that most attract radar-system designers are precision frequency tuning, phase offset control, and linear "chirp" capability.

This study discusses the option of incorporating DDS for use in a digital pulsed and/or frequency modulated continuous wave (FMCW) radar, and examined the necessary adaptations such as up-converting baseband signals from DDS to a radar transmission frequency, viable transmit and receive waveforms and the synchronization problem relating to synchronizing the many radiating elements that could range from a few to possibly thousands.

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I. INTRODUCTION

All warfare is based on deception…

…Secret operations are essential in war; upon them the army relies to make its every move…

Sun Tzu

A. MOTIVATION

Aegis has been regarded as the most competent naval warship in the US Navy today, known for its exceptional capability to perform a wide range of missions that includes providing anti-cruise missile protection for the naval task group, to anti-ballistic missile protection for US and its allies. With all great capabilities, the Aegis owes its naval superiority, in a large part, to its advanced AN/SPY-1 radar. The computer controlled AN/SPY-1 phased array radar brings together different radar functions such as search, detect, track, and guidance control all into one single system. Unlike conventional radar which is mechanically rotated to cover 360 degrees, the AN/SPY-1 radar has four huge fixed arrays to provide the 360 degrees continuous radar coverage as well as enhanced tracking capability on multiple tracks.

The drawback on AN/SPY-1 radar however, is the limitations by its legacy microwave plumbing and sources (with its original design dating back to 1960s) which confines the placement of the transmit/receive elements of the array. They needed to be co-located on a plane, and to get the required coverage there had to be four massive planes. This not only uses an enormous amount of the already limited ship's surface area, but also interrupts the smooth facade of the ship structure, which is a critical consideration for today's stealthy ship design. The heavy array faces complicate the structural design of the deckhouse, especially if composite materials are being used.

For a solution to the problem, a paradigm shift in radar system and antenna design is essential. Radar designers must find creative means of achieving the required radar performance without compromising the ship's stealthy characteristics. In its plainest form, it is a question of how to design the radar around a stealthy ship.

B. CONCEPT OF OPPORTUNISTIC ARRAY RADAR

Instead of letting the radar array dictate the ship's structure, why not let the ship's structure dictate where the elements of the array can be placed? This revolutionary idea could provide the potential of using the entire length and width of a large ship as the aperture for the radar that can be used for various purposes such as communication, surveillance, guidance and control, and even threat imaging. This idea of having integrated array elements in the ship's hull forming the aperture for the radar has recently been referred to as "an aperstructure opportunistic array radar".

Figure 1 illustrates the random placement of array elements across a DD(X) like platform [1]. The design of such an "opportunistic" phased array radar system that covers the entire length of a large ship involves the controlling of potentially many transmit and receive (T/R) elements that could range in the hundreds to the thousands. One particular application of interest is the ballistic missile defence (BMD). The operating frequency for the simulation in Figure 1 is 300 MHz.

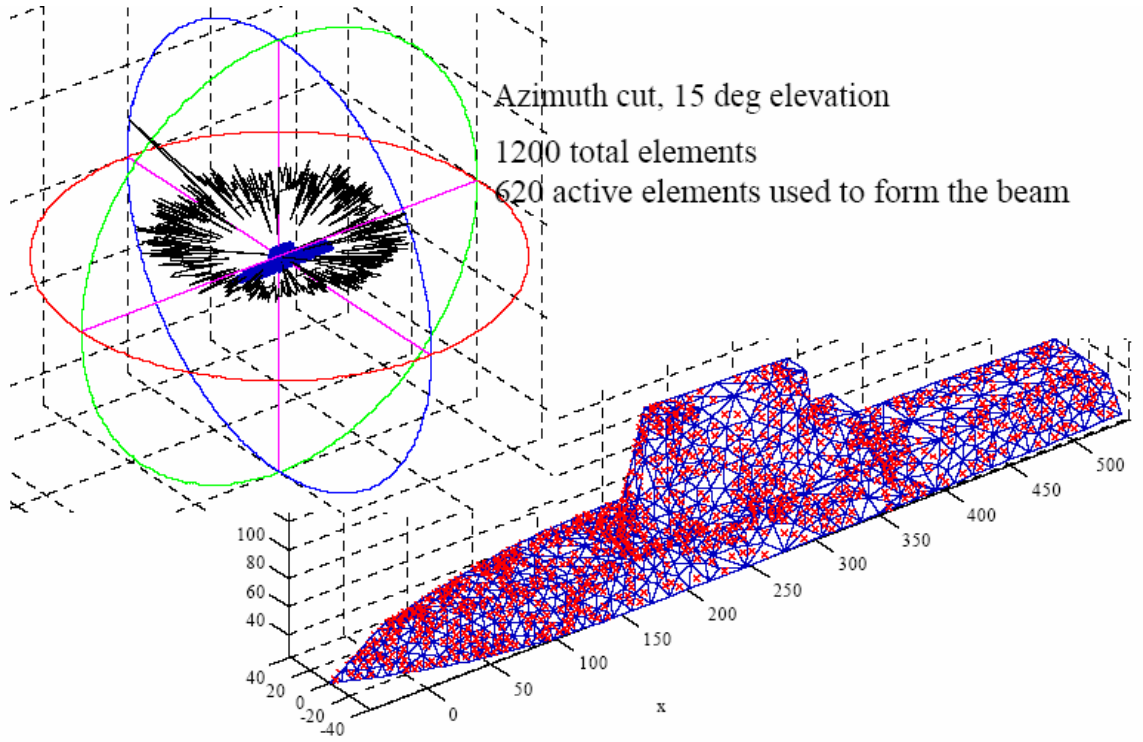


Figure 1. Ship model for the array and simulated pattern [a red × denotes an element location] (After Ref [1].)

With this many T/R elements that are randomly placed across the entire ship's façade, the approach requires a complete paradigm shift from conventional radar system design.

For a start, the T/R modules need to be freed from their present constraint. This means replacing the conventional radio frequency (RF) phase shifter, RF numeric controlled attenuator and microwave channeling that are bounding T/R elements together. This would require a large number of specially designed and integrated components that can self-synchronize with other elements and synthesize, modulate and demodulate radar waveforms.

This radical approach demands *Direct Digital Synthesis*, which is a digital means of producing an analog waveform, usually a phase or amplitude modulated sine wave, by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. Because waveform generations are primarily digital, it does not need waveguides as in the conventional analog waveform generators hence alleviating the constraint of requiring the antennas to be co-located together or near the waveform generators.

However, to be truly randomly locatable anywhere on the ship's superstructure, it is desirable that the digital T/R elements not be physically connected to the radar's centralized controller in any form, hence further removing the limitations bounded by maximum cable length, deck penetration, etc. Without the physical connection, the new digital T/R elements would have to be synchronized-and-controlled wirelessly by the radar's main controller that might be over a hundred meters away. Figure 2 depicts the concept of how such a wireless digital T/R module that can be connected to the radar's digital beam former and controller via a wireless transmission medium.

Like the AN/SPY-1 the ultimate desire is for the proposed aperstructure opportunistic array radar to be able to perform various radar functions such as search, detect, track, and guidance control simultaneously, however for the sake of simplicity, the initial research focus will be on the radar's ability to conduct long range ballistic missile defence (BMD) related functions such as search and detect.

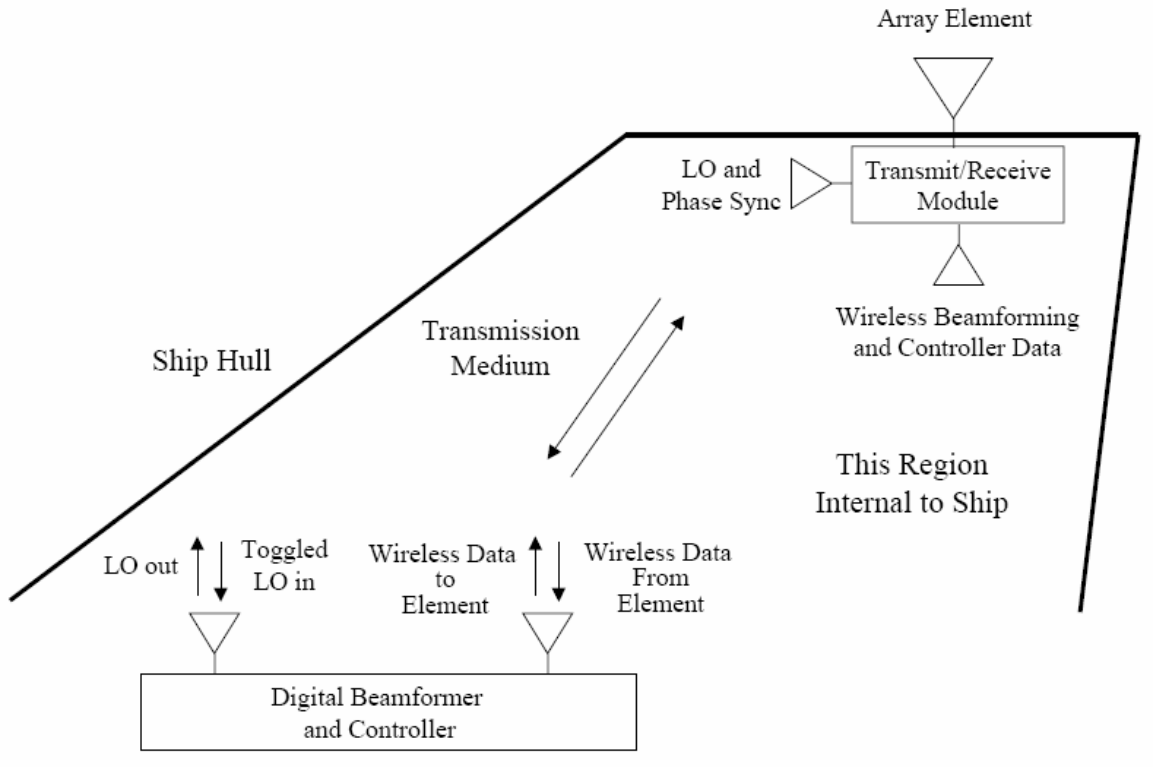


Figure 2. Block diagram of the proposed digital wireless array architecture.

This demanding concept is stretching today's technology and could potentially be astronomically costly if new technology or special components have to be developed. With the rapid technology advancement and cost reduction that can be offered by commercial-off-the-shelf (COTS) electronic components, it would be worthwhile to explore the use of commercially available digital waveform synthesizers and modulators for demonstrating the working concept of the proposed digital transmit and receive module, so as to keep costs to a minimum while maintaining high quality radar performance. For the purpose of our concept demonstration, it is more economical to construct a 2.4 GHz prototype radar versus the actual desired 300 MHz radar which is typical for long range BMD radar, since most of the commercially available products are optimized for use within this commercial frequency band. The concepts demonstrated using 2.4 GHz are directly applicable to other frequency bands.

C. DIGITAL TRANSMIT AND RECEIVE MODULE

The main idea behind the wireless digital T/R module is to replace the conventional radio frequency (RF) phase shifter with the digital phase shifting function of the direct digital synthesizer (DDS), and to replace conventional RF numeric controlled attenuator with the amplitude control function of the DDS.

In a digital transmit module, the beam forming and the waveform generation are combined. With the advancement in DDS technology, high precision of phase, amplitude and frequency is achievable with a DDS. However, because of limitations imposed by the sampling, present DDS can only produce low frequency signals (< 300 MHz), and therefore, it cannot directly produce signals in higher radar frequency bands.

The proposed wireless digital T/R module is made up of a transmitting and receiving module as shown in Figure 3 which is similar to the conventional T/R module. However, the adjustment of the amplitude and phase in the digital T/R module is realized in the DDS. Therefore, the linearity of the amplitude and phase of the frequency upconversion is critical to the generation of the final transmit beam. In other words, the amplitude and phase errors of the RF signal introduced from the low frequency signal whose amplitude and phase are controlled by the DDS should be as low as possible. That is the key difference between the transmit module of the digital T/R module to that of the traditional T/R module.

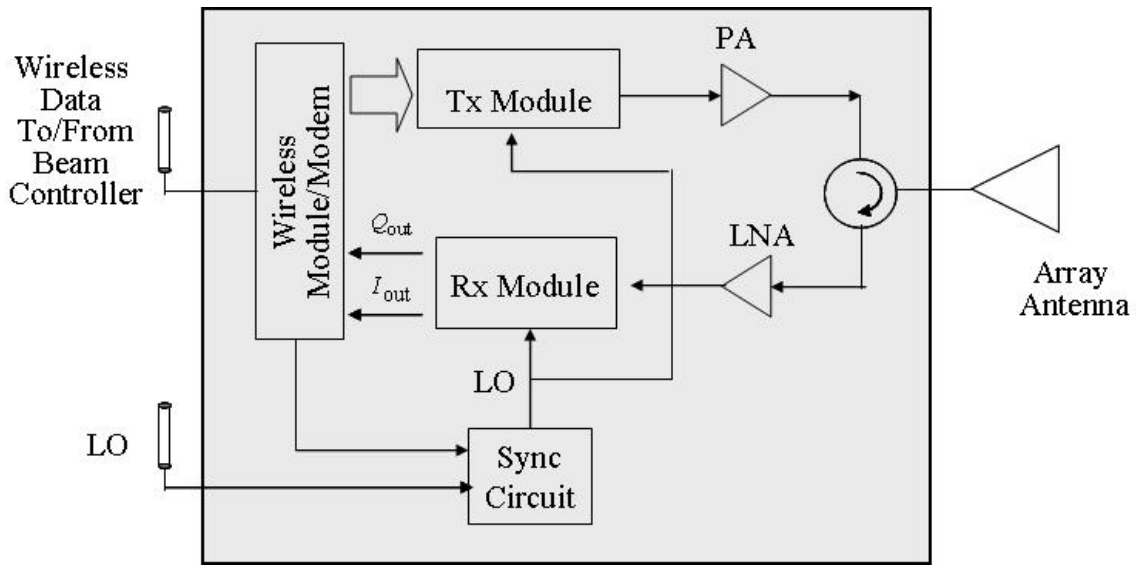


Figure 3. Concept of wireless digital T/R module.

In the transmitting state, the DDS produces the required waveform, which is then upconverted into the transmitted signal through single-stage frequency upconversion as shown in Figure 4. Section B of Chapter II will further describe the upconversion process and the required hardware.

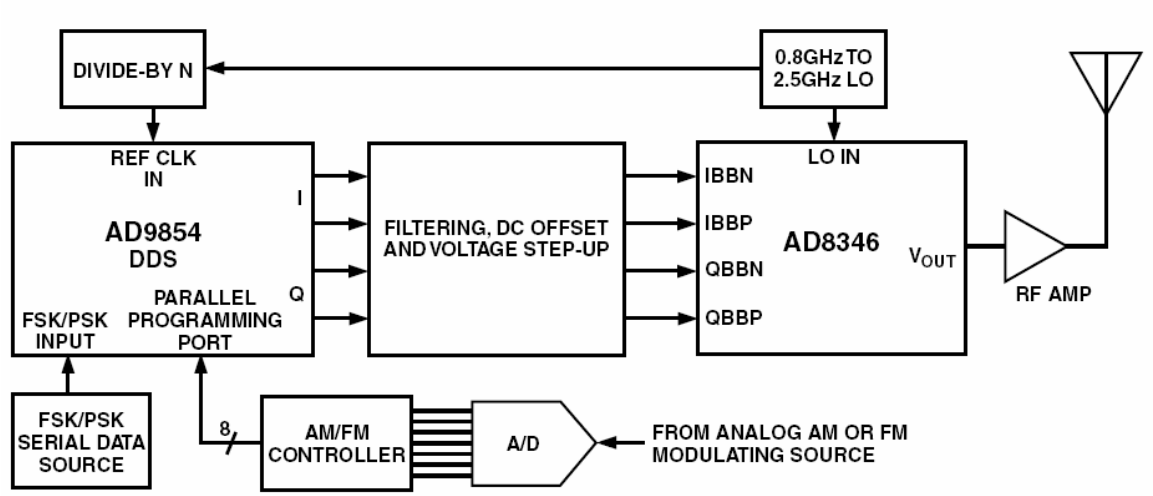


Figure 4. DDS/Modulator digital transmit module. (From Ref. [2].)

D. PREVIOUS WORK

This thesis is a continuation of the design and development of a three-dimensional 2.4 GHz digital phased array radar, for use in demonstrating the new aperstructure opportunistic array radar concept.

The transmit antenna design was carried out by Naval Postgraduate School (NPS) student LCDR Lance C. Esswein, USN [3]. Esswein had designed a phased array transmit antenna using COTS components and demonstrated that the genetic algorithm program and its pattern builder function would form a radiation beam in agreement with the theoretical calculations. The receiver architecture was investigated by another NPS student Eng Cher Shin, Ministry of Defense, Singapore [4] using COTS products and further researched by Ong Chin Siang, Ministry of Defense, Singapore [5].

In [4], the bandwidth characteristics of the *Analog Devices* AD8346EVAL quadrature modulator board were investigated. It was shown that the modulator board is not able to provide wide instantaneous bandwidth. Reference [5] proposed a technique of

using different types of time-varying phase weights for a linear frequency modulated (LFM) signal to improve the phase distortion and increase the operating bandwidth of the phased array. A preliminary laboratory setup using COTS components was presented in [5] to implement the time-varying phase weights on the transmit side. The COTS components include a AD9854EVAL DDS and a AD8346EVAL demodulator board. The preliminary results showed that AD8346EVAL was not able to provide a suppression of 36 dB on the image signal and would need a band pass filter to remove the undesired signals.

E. OBJECTIVE OF THIS THESIS

This thesis focuses mainly on the digital transmit side of the module. The first objective was to re-verify the findings in [5] and identify potential means of achieving 36 dB image suppression. This task is followed by determining the feasible methods of generating frequency modulation continuous wave (FMCW) waveforms and pulsed waveforms from the proposed digital transmit module.

Subsequent investigations shall center on modeling the achievable theoretical waveforms for the proposed digital transmit module setup and verifying the expected waveforms with the actual measured waveforms.

The secondary objective will focus on exploring the potential means of synchronizing multiple DDSs. This is a requirement for synchronizing the potentially hundreds of elements of the array that could cover the entire surface of a large ship.

In addition, a study on the latest DDS technology was conducted to appraise any new DDS feature or characteristic that could be exploited to ease or improve the implementation of the array elements.

F. THESIS OUTLINE

Chapter II, Section A describes the design of the proposed digital transmit module and presents the general radar waveforms expected of the digital transmit module. Section B touches on the adaptation necessary to fulfilling pulsed and FMCW radar application. Section C discusses in detail the upconversion technique for synthesizing

microwave frequency and the expected results. Section D states the importance of synchronizing the many T/R elements and Section E highlights the key synchronizing requirements in synchronizing multiple DDS devices.

Chapter III, Section A discusses the Matlab simulation results with comparison to the measured results from the upconversion experiment. Section B presents the method of generating radar pulses and the Matlab simulated results for the different pulse width and their expected pulse spectrum. Section C compares the two possible ways of synchronizing multiple DDSs and recommends the one with the simplest and smallest design.

Chapter IV, Section A provides the general conclusion while Section B recommends the next steps for immediate or future follow-ups.

Appendix A documents all the Matlab codes developed for this thesis and related calculations. Appendix B shows the write-up on the market research that was conducted to appraise any new DDS feature or characteristic that could be exploited to ease or improve the implementation of the array elements.

II. CONCEPT AND THEORY FOR THE DIGITAL TRANSMIT MODULE

A. DESIGNING THE DIGITAL TRANSMIT MODULE (FOR THE CONSTRUCTION OF THE 2.4 GHZ RADAR)

1. Synthesizing Microwave Frequencies

Although DDS technology is advancing rapidly, direct synthesis of ultra-high frequency (UHF) and microwave output frequencies is not yet practical or economically feasible. At present even a state-of-the-art DDS can only produce signals up to the range of 400 MHz. For this reason DDS is routinely being incorporated with a phase-locked loop (PLL) or up-converted with a mixer.

Unfortunately, multiplication using PLLs compromises signal integrity, frequency resolution, and agility. Also, up-converting a double sideband (DSB) signal to single sideband (SSB) at a higher frequency, using a mixer, may require difficult or impossible output filtering as well as a high-quality fixed-frequency local oscillator (LO). Methods used to overcome these shortcomings usually result in the need for multiple PLLs or mixer/filter/oscillator stages.

Reference [5] proposed the use of an improved and economical approach to single stage upconversion to the frequencies from 800-to-2500 MHz, using *Analog Devices'* AD9854 *Quadrature Complete-DDS* and AD8346 *Quadrature Modulator* as shown in Figure 5. The up-converted suppressed-carrier, single sideband signal would have greater than 36-dB typical rejection of LO and undesired sideband frequencies over the entire frequency range. Moreover, all DDS signal qualities are preserved, while the unwanted products of upconversion are minimized with a typical 36-dB rejection.

For up-converting quadrature signals synthesized by DDS, the block diagram in Figure 5 shows how AD9854 output signals would be applied to the AD8346 differential "baseband modulation" inputs for SSB upconversion near the LO frequency. This upconversion technique will be further discussed in detail in Section C.

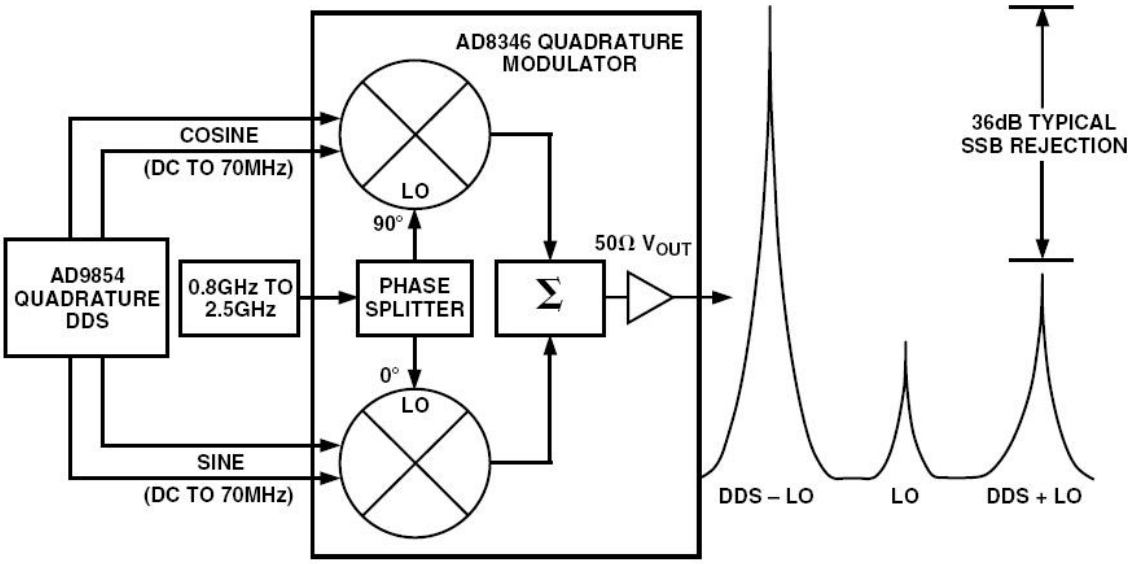


Figure 5. Quadrature DDS SSB upconversion. (From Ref. [2].)

2. General Waveforms and Impact on Radar Performance

The AD9854 DDS is capable of synthesizing various waveforms, which include triangular and square waves, but when used together with a quadrature modulator in the proposed setup as shown in Figure 5, the setup provides only a continuous sine wave type signal suitable for just a handful of CW and FMCW related applications. For other radar applications such as surveillance radar, it is necessary that the T/R element generates pulsed waveforms.

In this section the various waveforms and their properties are discussed. There are numerous options depending on radar requirement and the family of the widely used radar waveforms is summarized in Figure 6, each appropriate to a specific group of tasks.

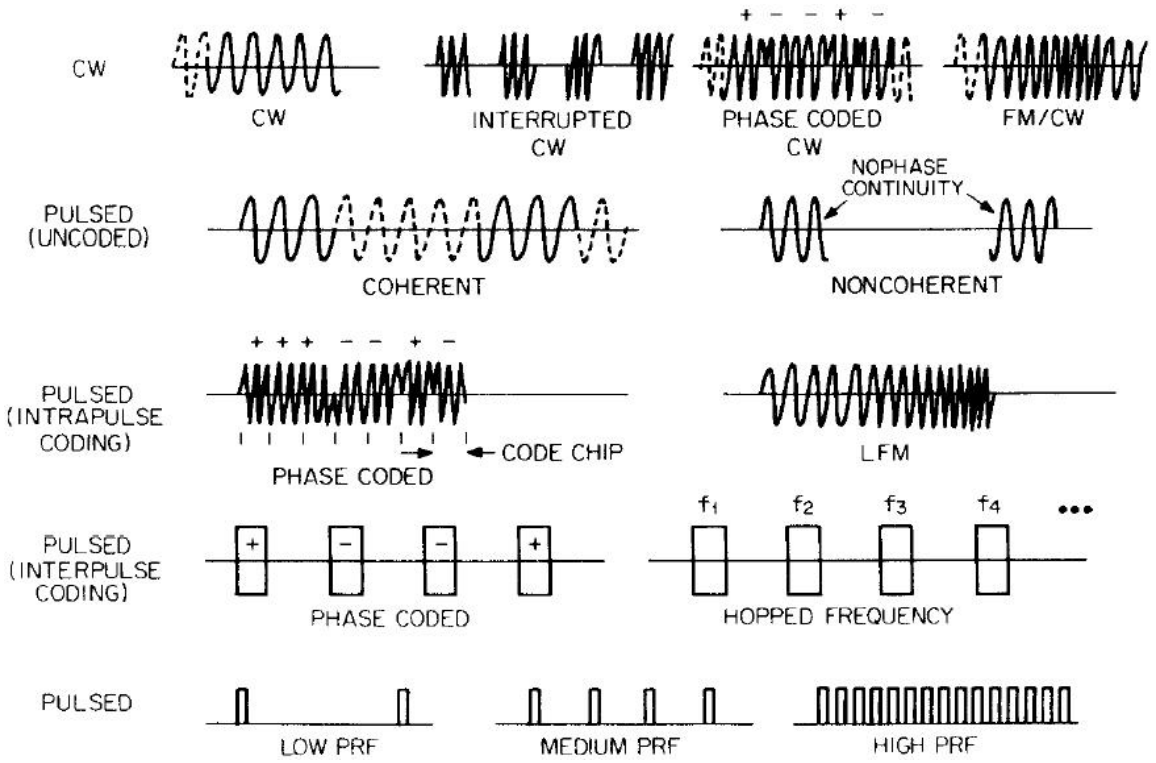


Figure 6. A partial listing of the family of radar waveforms. (From Ref. [6].)

On the top row is the continuous wave or CW waveform. These are most appropriate for applications where determining velocity is the main concern, where Doppler resolution of targets and clutter is critical and determining range is less crucial, such as in close-in range systems.

For applications where range resolution and accuracy are desired, pulsed waveform systems may be more appropriate. The pulsed waveforms may be coded or uncoded. These can be coded within a pulse (pulse compression) or from pulse to pulse. The coherent pulse-train waveform is almost always required for surveillance radars where some ranging is desired and high clutter rejection (>35 dB) is necessary.

Figure 7 illustrates the typical radar waveform structure commonly used in pulsed radar. The pulsed systems are typically categorized as low pulse repetition frequency (PRF) where range is unambiguous but Doppler may be ambiguous; medium PRF where both range and Doppler are likely to be ambiguous; and high PRF where range is ambiguous but Doppler is not.

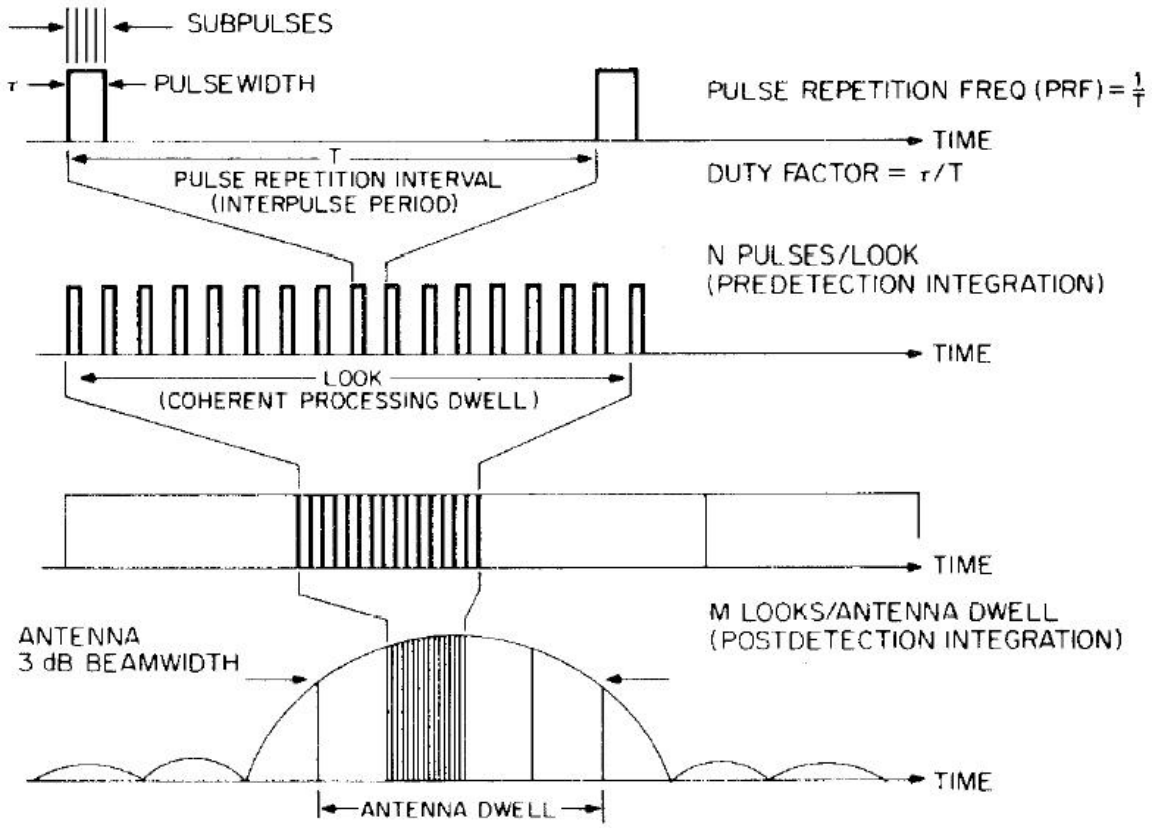


Figure 7. Pulse train radar waveform structure. (From Ref. [6].)

For application such as our 2.4 GHz multifunction prototype radar, the radar needs to be versatile in generating various CW and pulse typed waveforms that include frequency spreading. The frequency spreading includes two aspects: one is to spread the operating frequency; the other is to spread operating bandwidth. The operating frequency spreading is achieved by up-converting to higher frequency. While, the operating bandwidth spreading can be achieved through varying the DDS or LO frequency when the operating frequency is being up-converted.

B. ADAPTATION FOR PULSED AND FMCW RADAR APPLICATIONS

As commented earlier, the output from the setup in Figure 5 would be a CW type waveform with its frequency determined by the DDS operating frequency and the LO

frequency. To satisfy a pulsed requirement or to generate radar pulses, a separate on/off switching is required at the RF output to emulate pulsing. Figure 8 shows an adapted design of the setup for implementing as pulsed radar.

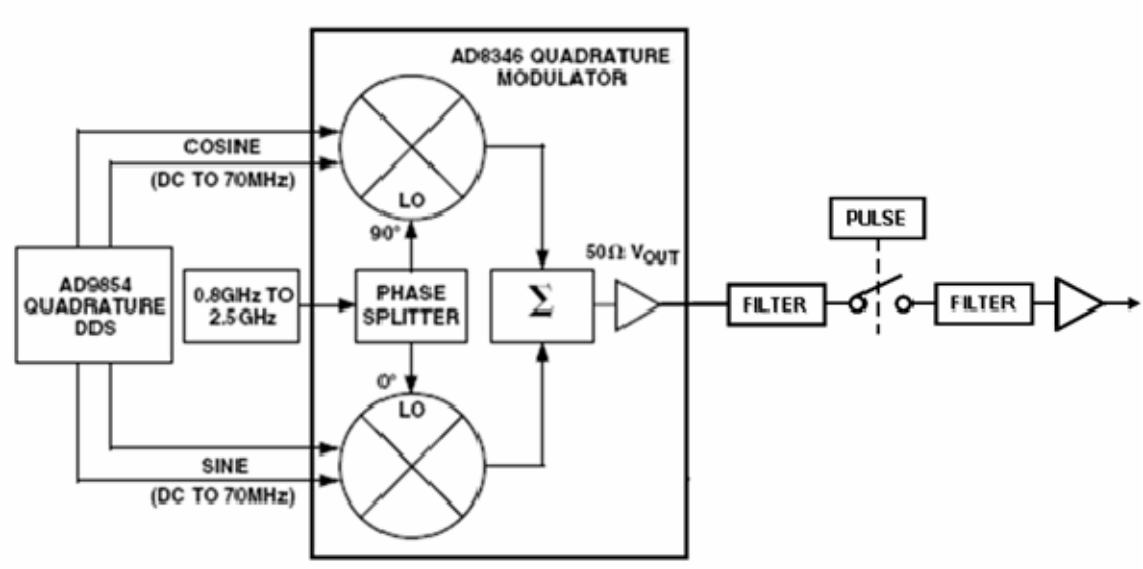


Figure 8. AD9854 DDS in pulsed radar applications. (After Ref. [2].)

The following paragraphs provide a general description and specification on the two key components for the proposed digital transmit module: the *Analog Devices* AD9854 DDS and the AD8346 *I/Q* modulator.

1. Direct Digital Synthesis (AD9854EVAL)

DDS is a digital means of producing an analog waveform. Because operations within a DDS device are primarily digital, it can offer fast switching between output frequencies, fine frequency resolution, and operation over a broad spectrum of frequencies. With advances in design and process technology, today's DDS devices are very compact and draw little power.

The AD9854 digital synthesizer from *Analog Devices* was investigated to determine its suitability for used in the construction of the 2.4 GHz prototype radar. Below is a brief description taken from reference [7]. It states:

The AD9854 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with two internal high-speed, high-performance quadrature D/A converters to form a digitally programmable *I* and *Q* synthesizer function. Figure 9 shows the functional block diagram of the AD9854 DDS and Figure 10 shows the actual board layout. When referenced to an accurate clock source, the AD9854 generates highly stable, frequency-phase amplitude-programmable sine and cosine outputs. The AD9854's circuit architecture allows the generation of simultaneous quadrature output signals at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second.

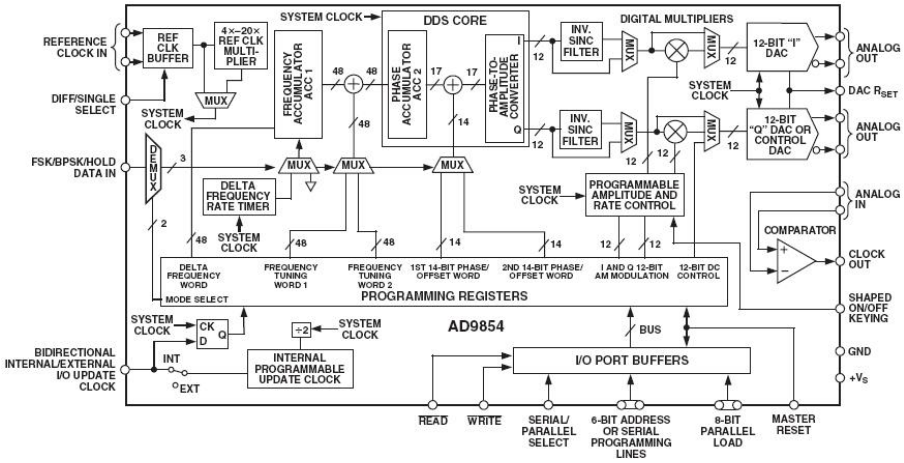


Figure 9. AD9854EVAL functional block diagram. (From Ref. [7].)

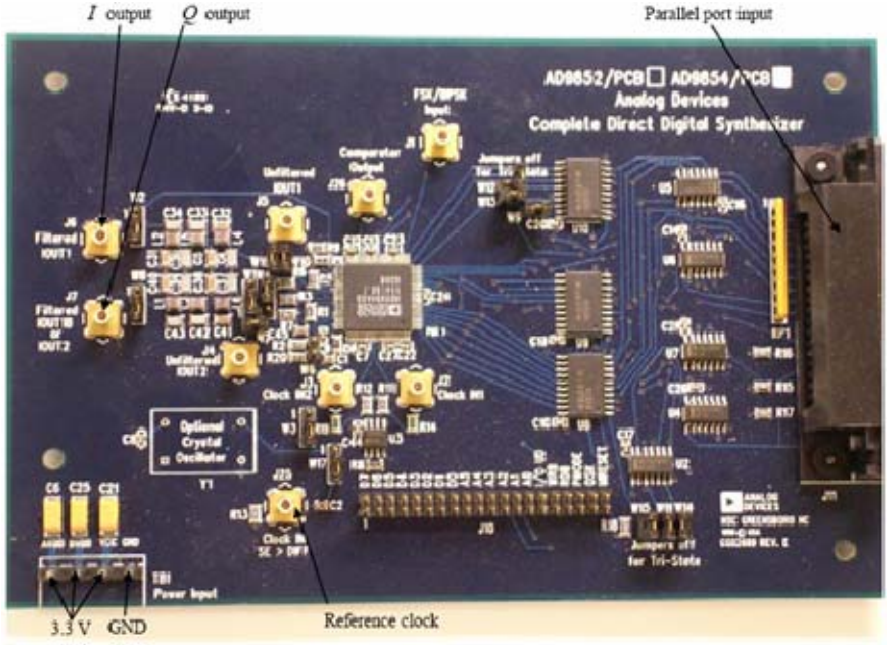


Figure 10. Picture of DDS AD9854EVAL board.

2. Quadrature Modulation (AD8346EVAL)

One modulation technique that lends itself well to digital processes is called "*I/Q* Modulation" (or “Quadrature Modulation”), where "*I*" is the in-phase component of the waveform, and "*Q*" represents the quadrature component.

In its various forms, *I/Q* modulation is an efficient way to transfer information, and it also works well with digital formats. An *I/Q* modulator can actually create amplitude modulation (AM), frequency modulation (FM) and phase modulation (PM). When modulating a carrier with a waveform that changes the carrier’s frequency slightly, one can treat the modulating signal as a phasor. It has both a real and an imaginary part, or alternatively, an in-phase (*I*) and a quadrature (*Q*) part. If a receiver is constructed so that it locks to the carrier, one can decipher information by reading the *I* and *Q* parts of the modulating signal.

For a narrowband signal, the representation for the carrier signal is

$$s(t) = A(t)\cos[\omega_c t + \varphi(t)] = I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t) \tag{1}$$

where

$I(t) = A(t)\cos(\varphi(t))$ is the in-phase component of $s(t)$,

$Q(t) = A(t)\sin(\varphi(t))$ is the quadrature component of $s(t)$,

$\omega_c = 2\pi f_c$, and f_c is the carrier frequency,

$A(t)$ is the amplitude of $s(t)$ and,

$\varphi(t)$ is the phase of $s(t)$

The amplitude $A(t)$ and phase $\varphi(t)$ of $s(t)$ can be found by

$$A(t) = \sqrt{I(t)^2 + Q(t)^2} \tag{2}$$

and

$$\varphi(t) = \tan^{-1}\left(\frac{Q(t)}{I(t)}\right) \tag{3}$$

The fundamental building blocks of a digital quadrature modulator are essentially the same as those for the analog single-sideband modulator as shown in Figure 11. An analog quadrature modulator mixes the message (or baseband radar waveform) with two

carriers. Both carriers operate at the same frequency, but are shifted in phase by 90 degrees relative to one another (hence the "quadrature" term). This simply means that the two carriers can be expressed as $\cos(2\pi f_c t)$ and $\sin(2\pi f_c t)$. The message, too, is modified to consist of two separate signals: the original and a 90 degree phase shifted version of the original. The original is mixed with the cosine component of the carrier and the phase shifted version is mixed with the sine component of the carrier. These two modifications result in the implementation of the single sideband function.

Section C will describe in detail the quadrature modulation technique involved in this particular application experiment.

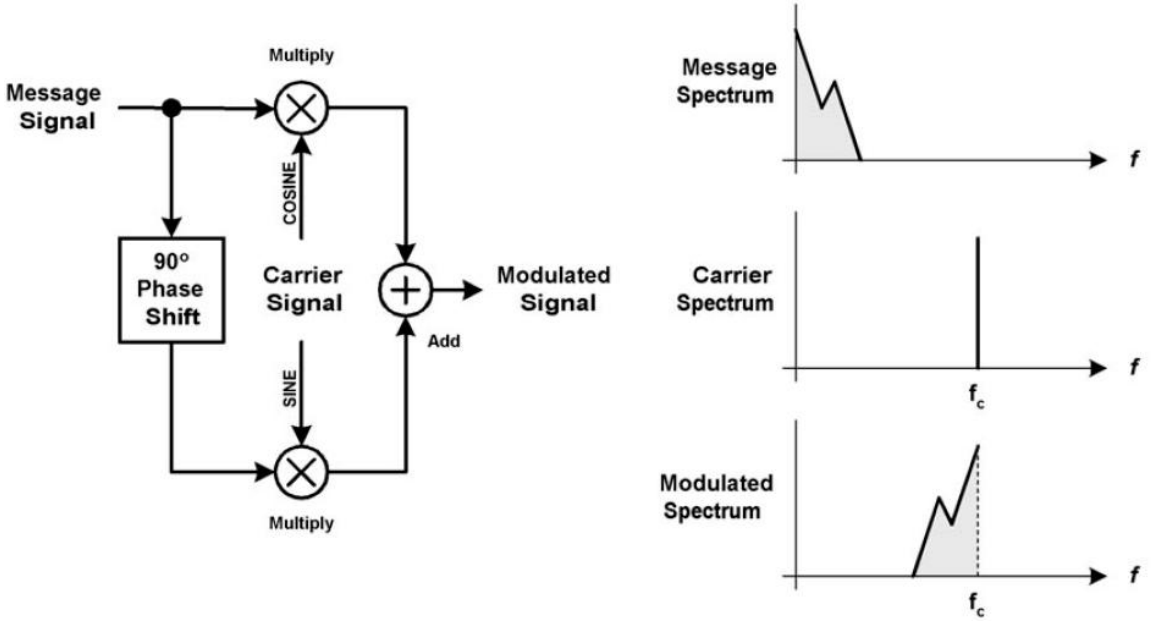


Figure 11. Single sideband modulation. (From Ref. [8].)

The AD8346 *I/Q* modulator from *Analog Devices* was investigated in this thesis to determine its suitability for use in the construction of the 2.4 GHz prototype radar. Below is a brief description taken from reference [9]. It states:

> The AD8346 is a *I/Q* modulator for use from 0.8 GHz to 2.5 GHz. Its excellent phase accuracy and amplitude balance allow high performance direct modulation to RF. Figure 12 shows the functional block diagram of the AD8346 modulator. The differential LO input is applied to a polyphase network phase splitter that provides accurate phase quadrature from 0.8 GHz to 2.5 GHz. Buffer amplifiers are inserted between two sections of the phase splitter to improve the signal-to-noise ratio (SNR).

The *I* and *Q* outputs of the phase splitter drive the LO inputs of two Gilbert-cell mixers. Two differential *V*-to-*I* converters connected to the baseband inputs provide the baseband modulation signals for the mixers. The outputs of the two mixers are summed together at an amplifier which is designed to drive a 50 Ω load.

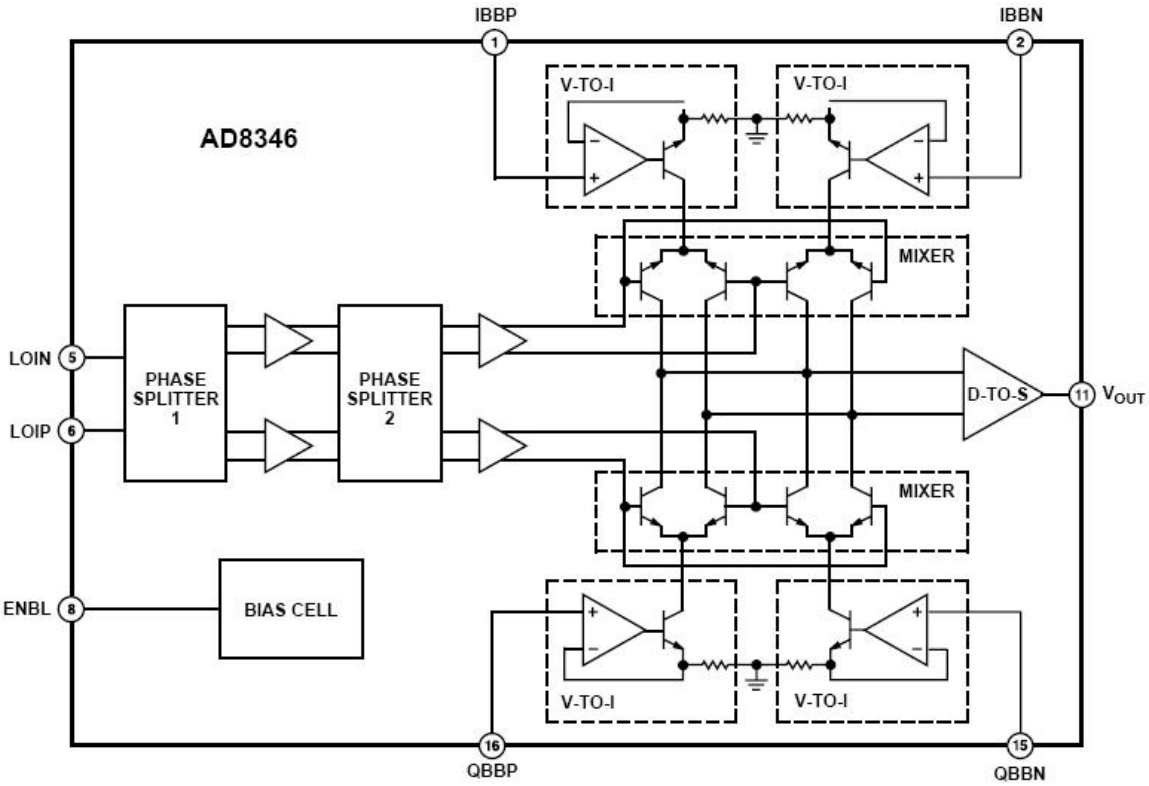


Figure 12. AD8346EVAL functional block diagram. (From Ref. [9].)

C. THE PROPOSED UPCONVERSION TECHNIQUE

1. General Mixing Theory

An option to upconvert a DDS signal to UHF/microwave frequencies is to incorporate the use of a mixer. Upconverting does not significantly increase either the spur levels or the phase noise. Furthermore, frequency agility and resolution remain unaffected. The largest obstacle to overcome is the presence of the double-sideband (DSB) output: $f_c + f_o$ and $f_c - f_o$, and any LO feedthrough that occurs. Figure 13, showing a 200-MHz region of spectrum of a suppressed carrier (LO), single-upconversion mixer output, demonstrates this problem with upconversion. The upper sideband is labeled USB; the lower sideband LSB.

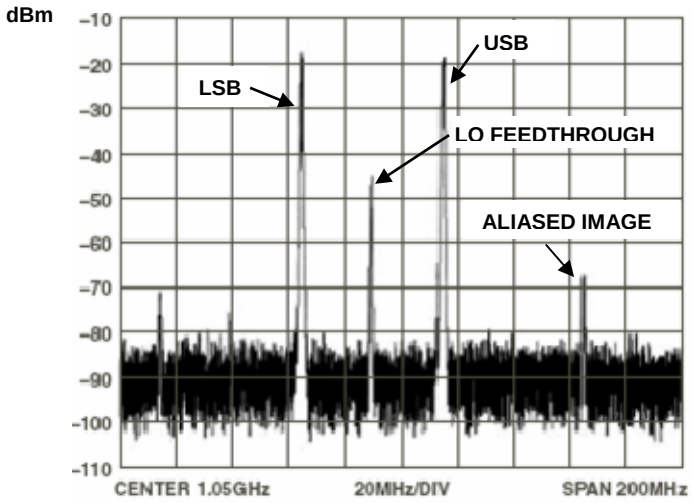


Figure 13. DSB output from typical mixer. (After Ref. [1].)

In quadrature upconversion, as shown in Figure 14, two mixers are driven with sine and cosine LOs, which are internally derived from an external single-ended high quality oscillator. The mixers are fed sine and cosine baseband signals (filtered DDS output signals) to be symmetrically up-converted about the fixed LO. The two mixer outputs are summed internally to add in-phase components and reject quadrature components of the mixer outputs. The end result (without additional filtering) is a suppressed-carrier, single side band, voltage output at –10 dBm and 50-ohm impedance, at a frequency that is either the sum or difference of the LO and baseband signals.

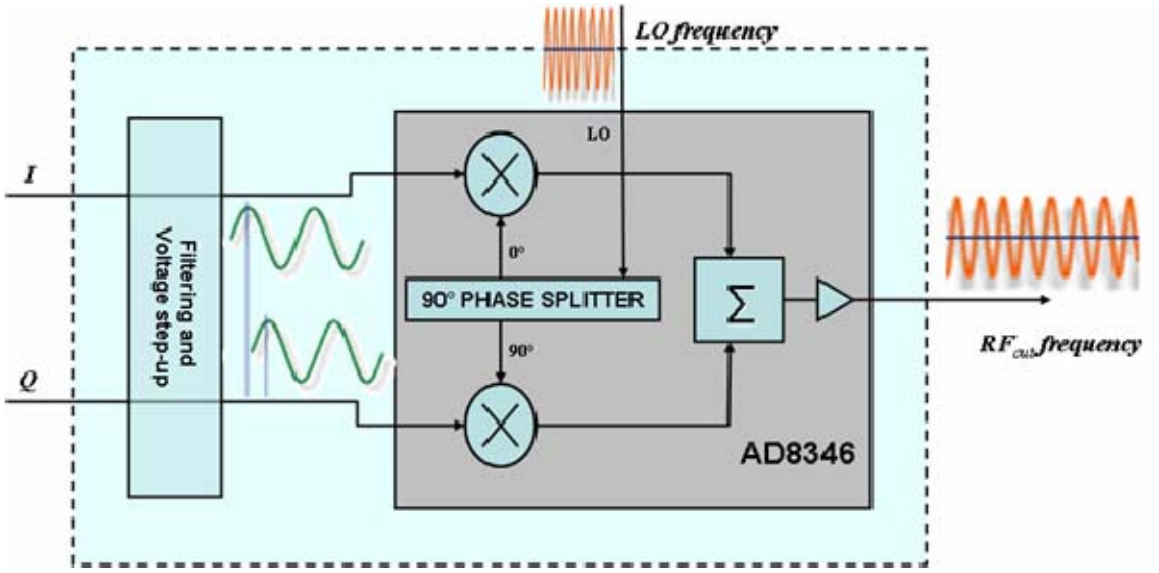


Figure 14. Quadrature upconversion using the AD8346.

2. LO Feedthrough

In reality however, there will be some remnants of the LO present in the output port. This is known as LO feedthrough. LO feedthrough will occur from the LO port to output port due to parasitic capacitance, power supply coupling, etc. LO feedthrough that is co-located with a carrier or present at the location of an out-of-channel measurement will have effects similar to those experienced with baseband carrier images. LO feedthrough can be minimized by adjusting *I* and *Q* offset, and *I/Q* quadrature skew.

3. Opposing Sideband

In addition to the LO feedthrough, there is also a high probability that an opposing sideband is present at the output. This is because errors in the *I* and *Q* quadrature phase relationship are introduced after the signals exit the AD9854 integrated chip (IC). This is due to the filters, unequal cable and PCB trace lengths, transformer differences, etc. Amplitude inequalities will also contribute to the inadequate suppression of the unwanted sideband.

Phase errors can be minimized by adjusting cable lengths from the AD9854 to the AD8346 evaluation board. Amplitude inequalities can be corrected using the AD9854's 12-bit, independent sine and cosine (*I* and *Q*), digital amplitude multiplier stages.

4. Proposed Laboratory Setup

A quadrature implementation of the SSB upconverter was accomplished by [1] using the AD9854 DDS and the AD8346 *I/Q* modulator evaluation boards. Modifications to the AD8346 evaluation board were required to accept the filtered, quadrature, single-ended signals provided by the AD9854 evaluation board. The output voltage levels also needed to be increased to suit the AD8346 input requirements. A diagram of the lab hook-up and modifications is seen in Figure 15. Descriptions on the additional components as proposed by [1] are as follows:

1. Add two 1:16 center-tapped impedance-step-up transformers (Mini-circuits T16-6T) to convert single-ended quadrature signals to differential signals and to provide a 1:4 voltage step-up. Use of the center-tapped secondary allowed a dc offset voltage of 1.2 volts to be added to the differential signals to comply with the AD8346 input-biasing requirements.
2. Add 1000-ohm termination resistors across each transformer output.
3. Add a 1.2-volt dc bias source consisting of two silicon diodes forward-biased from the 3.3 volt supply voltage through a 2000-ohm current-limiting resistor. Connect to center-tap of both *I*- and *Q*-channel transformer secondary windings.

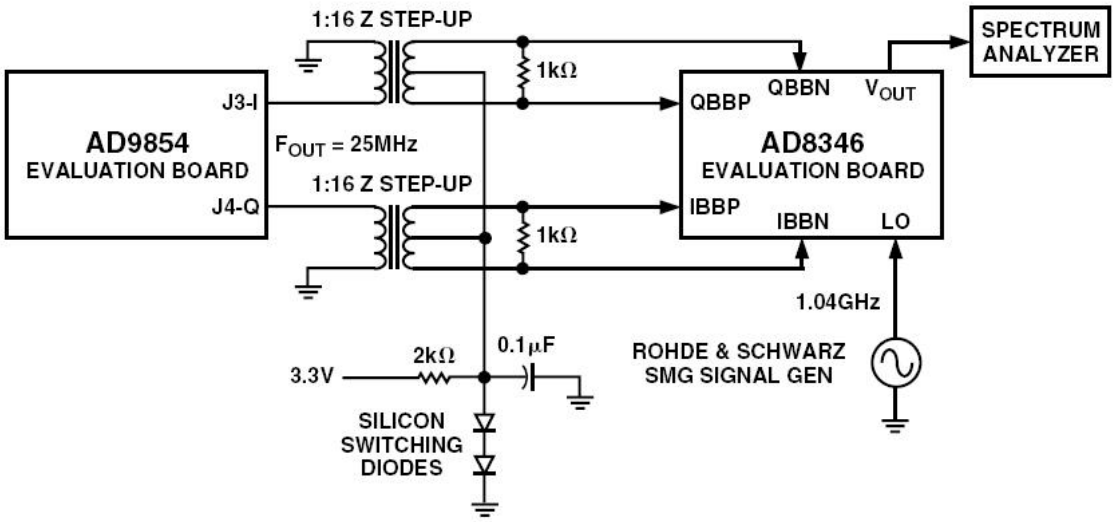


Figure 15. Recommended lab setup for SSB upconversion. (From Ref. [2].)

For our lab experiment, a printed circuit board (PCB) for the step-up transformer was designed based on the schematic diagram shown in Figure 16. The PCB was fabricated by Electronic Controls Design Inc. and the material used is FR-4, a standard glass epoxy substrate. Figure 17 shows that PCB board diagram as well as the actual fabricated board of the step-up transformer with two subminiature version A (SMA) connectors for the quadrature output signals from AD9854EVAL, and four SMA connectors for the IBBN, IBBP, QBBN and QBBP input signals of the AD8346EVAL.

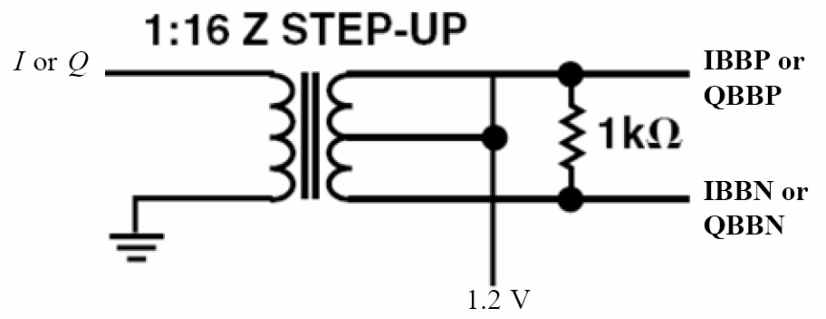
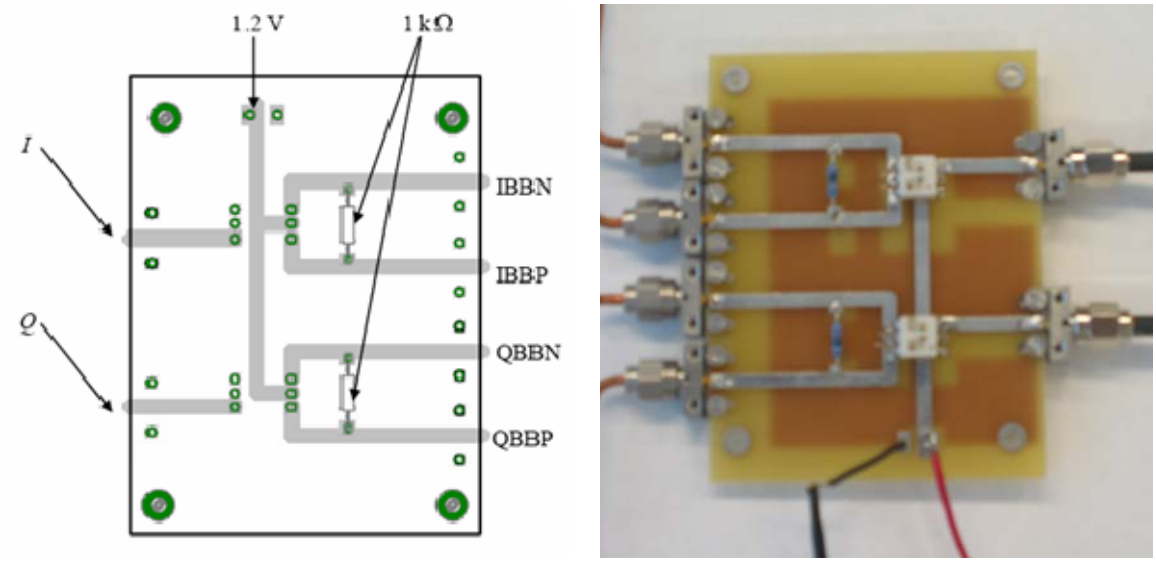


Figure 16. Schematic diagram of center-tapped impedance step-up transformer. (After Ref. [2].)



(a) Board routing diagram (b) Actual fabricated board

Figure 17. Step-up transformer PCB.

5. Expected Results

Figure 18 shows a 200-MHz segment of the output spectrum of the AD8346 centered around 1.05 GHz. The DDS "modulating" upper and lower sideband signals are seen 25 MHz away on either side of the LO at 1.04 GHz. A difference of –40 dB is indicated between the suppressed upper sideband (USB) and the favored lower sideband (LSB) amplitudes. The 40-dB differential equates to a power ratio of about ten-thousand to one. This level of sideband suppression is indicative of approximately 1 degree of input-signal phase mismatch. Note that the LSB frequency ($[f_c - f_o]$ or $[f_{LSB}]$) would be the transmitted radar frequency.

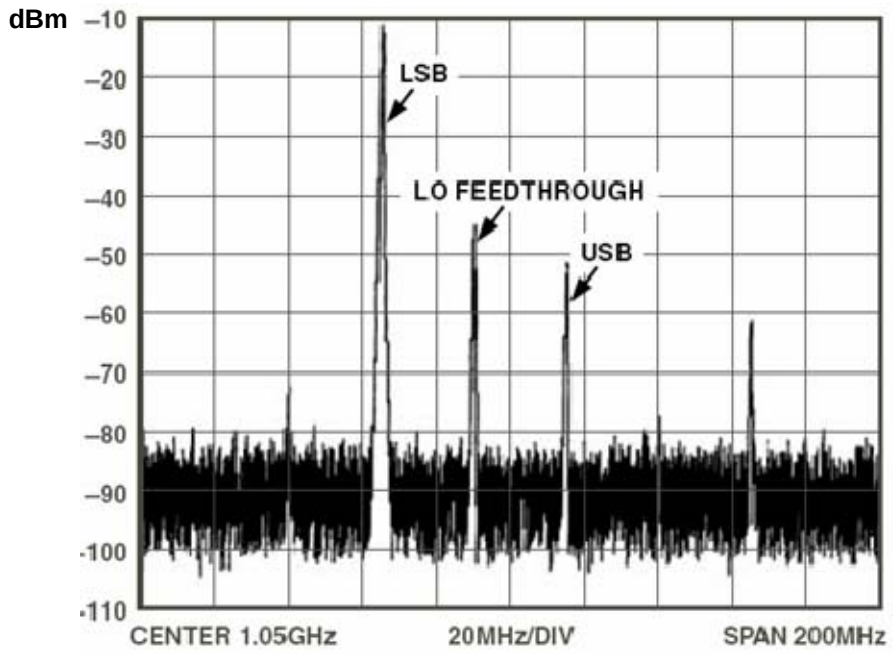


Figure 18. Spectrum analyzer output of the experimental setup in Figure 17. (From Ref. [2].)

The measured result from the upconversion lab experiment is presented in Section A of Chapter III.

D. SYNCHRONIZING MULTIPLE T/R MOUDLES

In opportunistic phased array radar, the elements are located randomly across a huge area that may cover the entire length and width of a large ship. This may give rise to potentially many hundreds of T/R elements. Each T/R element would have to work in synchronous harmony with others to electronically steer the radar beam. This can be achieved by assigning a single DDS device (or channel) to each individual antenna (or T/R) element. The phase adjustments by the individual DDSs would be the mechanism for steering the beam.

From a more technical point of view, the use of DDS, modulator and demodulator in each T/R element would require precise phase-synchronization of multiple synthesized RF output signals to one another. This requirement includes the synchronization of 1)

Reference clock [REFCLK] signals and 2) Local oscillator [LO] signals to each of the potentially hundreds of T/R modules.

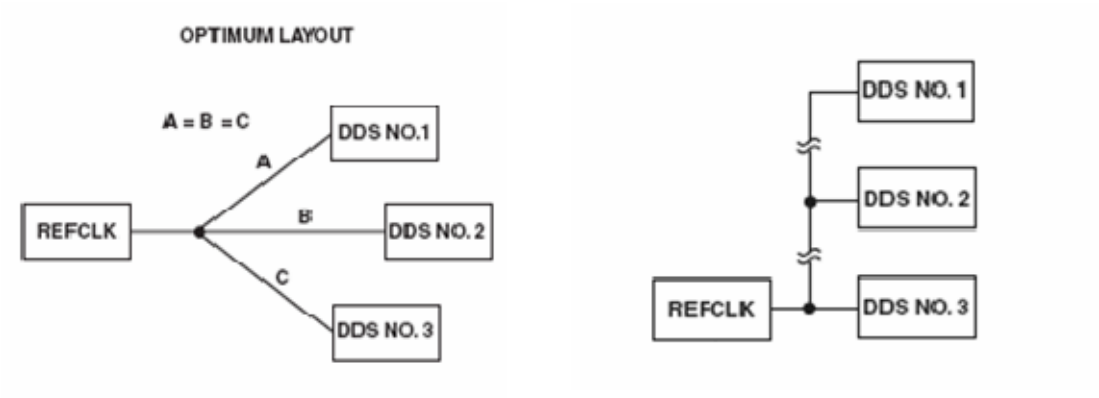
The ultimate goal, which is also the main challenge, is to implement this synchronization of T/R modules "wirelessly," since this is the key to realizing the aperstructure opportunistic array radar concept. The approach to synchronization of multiple DDS devices is discussed in this thesis and the synchronization of the LO signal is an on-going research topic that is addressing the synchronization techniques discussed here.

E. SYNCHRONIZING MULTIPLE DDSs

Phase synchronization of multiple synthesizers is a challenge for PLL and other traditional analog-based architectures. The AD9852/9854 and AD9850/9851 DDS devices from *Analog Devices*, with up to 14 bits of programmable phase-offset resolution (for AD9852/9854), provide the possibility for phase synchronization of multiple synthesized signals. The synchronization of multiple DDS devices can be accomplished as follows.

There are two basic timing requirements to be met in order for successful synchronization of the DDS to occur. The first, and somewhat obvious, is a coincidental REF clock between all DDSs. Coincidental means that the REF clock pins of each DDS have REF clock timing coincident in time as illustrated in Figure 19. This is accomplished through proper circuit layout.

The second timing requirement between all DDS devices is the coincidental transfer of the programmed input data to the DDS core. Performing this transfer is a key signal: the I/O update clock for the AD9854/9852. If the rising edge of this signal is sent synchronously to the multiple DDSs, along with proper set-up time relative to the REF clock, then synchronization can be achieved.



(a) Parallel distribution (b) Serial distribution

Figure 19. The parallel method is the optimum REFCLK circuit layout for synchronizing DDSs.

The wired distribution network shown in Figure 19 can be replaced with wireless channels. For example a modulated pulse train could be transmitted from REFCLK. An envelope detector at each DDS would extract the pulse train envelope, which is used for synchronization. Section C of Chapter III will provide more details on the technique(s) to achieving DDS synchronism.

F. SUMMARY

This chapter presented the method to synthesize a microwave frequency using present DDS technology and delved into the types of waveforms that can be generated by the DDS versus those expected from a typical radar transmit module. It proposed the necessary adaptation needed to satisfy radar applications such as surveillance and ballistic missile defense.

This chapter also provided a detailed description on the recommended upconversion technique and discussed the theory, results and cause of the undesired products from the upconversion. It had a technical description of the DDS AD9854 and the AD8346 *I/Q* modulator and with a discussion of how they can be setup to form part of the wireless transmit module.

Finally, the potentially big challenge in an opportunistic radar was addressed: how to synchronize the potentially many T/R elements that could cover an area that is as huge as a destroyer ship? The key requirements that have to be satisfied in order to achieve successful synchronization were discussed.

III. EXPERIMENT AND CONCEPT ANALYSIS

A. UPCONVERSION TO 2.4 GHz FREQUENCY

Depending on the radar frequency band, it may be necessary to frequency shift the waveform spectrum up to a carrier. To demonstrate this process in the lab, a carrier frequency of 2.4 GHz is selected for convenience.

The key objective of this experiment is to re-verify the previous finding reported in [5]. The first step is to re-verify using Matlab simulation to determine if the 36 dB suppression reported in [2] is indeed achievable by the proposed hardware setup previously discussed in Section C.4 of Chapter II.

The approach to this experiment is divided into two sub tasks. The first is to analyze the theoretical (computed) waveforms at various stages from the input to the output. This is done by analyzing the hardware setup as presented in Figure 20 and later modified as shown in Figure 8 for the pulse waveform analysis. The theoretical data were computed using Matlab software; the computed data were later compared to the measured results to ensure that the results were in agreement with the analysis.

The subsequent task was to set up the experiment as proposed by [5] with the AD9854, AD8346, a newly fabricated transformer PCB and other measuring instruments.

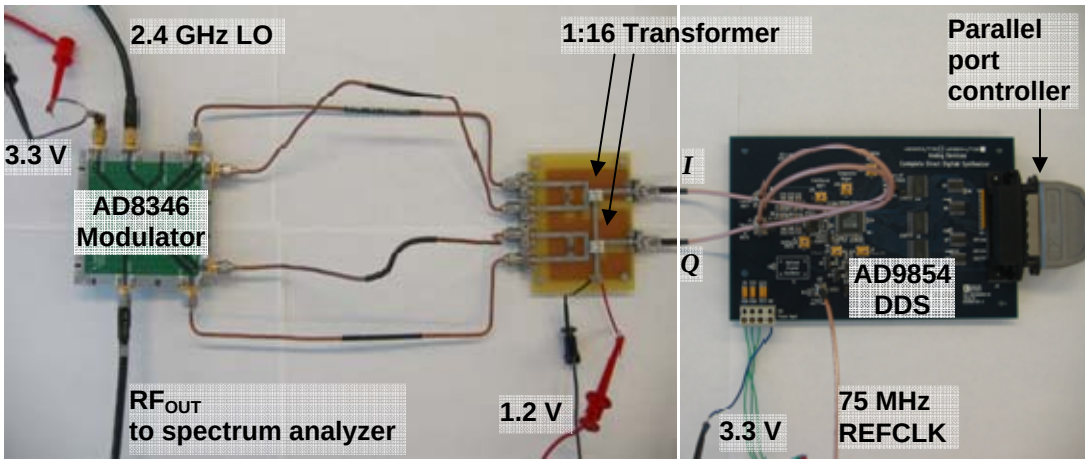


Figure 20 Laboratory setup for upconversion.

The experiment was carried out mainly with an LO frequency of 2.4 GHz and a DDS operating frequency ranging from 1 MHz to 25 MHz. The raw results were then measured and collected.

1. Matlab Calculation

From the quadrature upconversion as shown in Figure 5, the waveforms at various stages throughout the upconversion could be analyzed using Matlab program. The Matlab software version used for the simulation is version v6.5.1.

In the quadrature conversion setup, two mixers are driven with sine and cosine LOs (i.e. with 90 degree phase difference from one another). The mixers are then fed with sine and cosine baseband signals (filtered DDS output signals) to be symmetrically up-converted about the fixed LO, which produce the following equations:

$$I_{signal} = \sin\left(\omega_o t\right)\sin\left(\omega_c t\right) \tag{4}$$

$$Q_{signal} = \cos\left(\omega_o t\right)\cos\left(\omega_c t\right) \tag{5}$$

where ω_o is the angular frequency derived from $2\pi f_o$ and $\omega_c = 2\pi f_c$
f_o is defined as the DDS operating frequency
f_c is defined as the LO frequency

The two mixer outputs are then summed internally to add in-phase components and reject quadrature components of the mixer outputs. This gives rise to the equation

$$V_{out} = I_{signal} + Q_{signal} \tag{6}$$

or

$$V_{out} = \sin(\omega_o t)\sin(\omega_c t) + \cos(\omega_o t)\cos(\omega_c t) \tag{7}$$

The end result (without additional filtering) is a suppressed-carrier, single sideband, at a frequency that is the difference between the LO and baseband signals (i.e. $f_c - f_o$).

LO leakage - However, in practice, there will always be imperfection in the system that creates unwanted signals that appear at the output (and seen on a spectrum analyzer) that are not yet taken into account in this simple theoretical model. To be precise, in the model prediction we have to assume that there is going to be a slight

voltage offset, V_{OSBB} in one of the baseband (*I/Q*) input circuits due to reasons described in Section C.2 of Chapter II. The above equation can be re-written to include this offset and the equation would then become

$$V_{out} = (\sin(\omega_o t) + V_{OSBB})\sin(\omega_c t) + \cos(\omega_o t)\cos(\omega_c t) \tag{8}$$

Simplifying further yields

$$V_{out} = \sin\left[(\omega_o - \omega_c)t\right] + V_{OSBB}\sin(\omega_c t) \tag{9}$$

Now there is a component of the output signal at the LO frequency, namely V_{OSBB} $\sin(\omega_c.t)$. This is commonly referred to as the LO feedthrough phenomenon. From the specification of AD8346 quadrature modulator, it is stated that the LO feedthrough is typically at –42 dBm. This is around –29 dBc (dB relative to the carrier) since the typical carrier output power for AD8346 is around –13 dBm. Including this figure into the equation gives V_{OSBB} to be

$$V_{OSBB} = 10^{\frac{-29}{20}} = 0.0355 \tag{10}$$

The equation (9) then becomes

$$V_{out} = \sin[(\omega_c - \omega_o)t] + 0.0355\sin(\omega_c t) \tag{11}$$

If this unwanted LO feedthrough component is either at or very close to the desired output signal, RF filtering will not be possible.

***I/Q* imbalance** – Baseband *I/Q* amplitude imbalance and imperfect quadrature and amplitude imbalances at the outputs of the phase splitter create unwanted sideband interferers. Typically a 0.2 dB amplitude imbalance and 1° phase imbalance can be expected from phase splitter outputs that results in upper sideband amplitude of –36 dBc (note that the size of this component is proportional to the output power of the desired signal).

The complete Matlab code for generating the following results can be found in APPENDIX A. The LO frequency (f_c) to be used for the calculations is set at 2.4 GHz and the DDS operating frequency (f_o) is set at 20 MHz. From the Matlab calculation, it can be seen that the opposing sideband can be suppressed significantly. Figure 21 shows

the results of the calculation. It seems that if the phase error is as reported in [2] to be around 1 degree of the signal, then it is very likely that the suppressed sideband should be able to achieve the reported 36 dBc suppression as compared to the desired LSB.

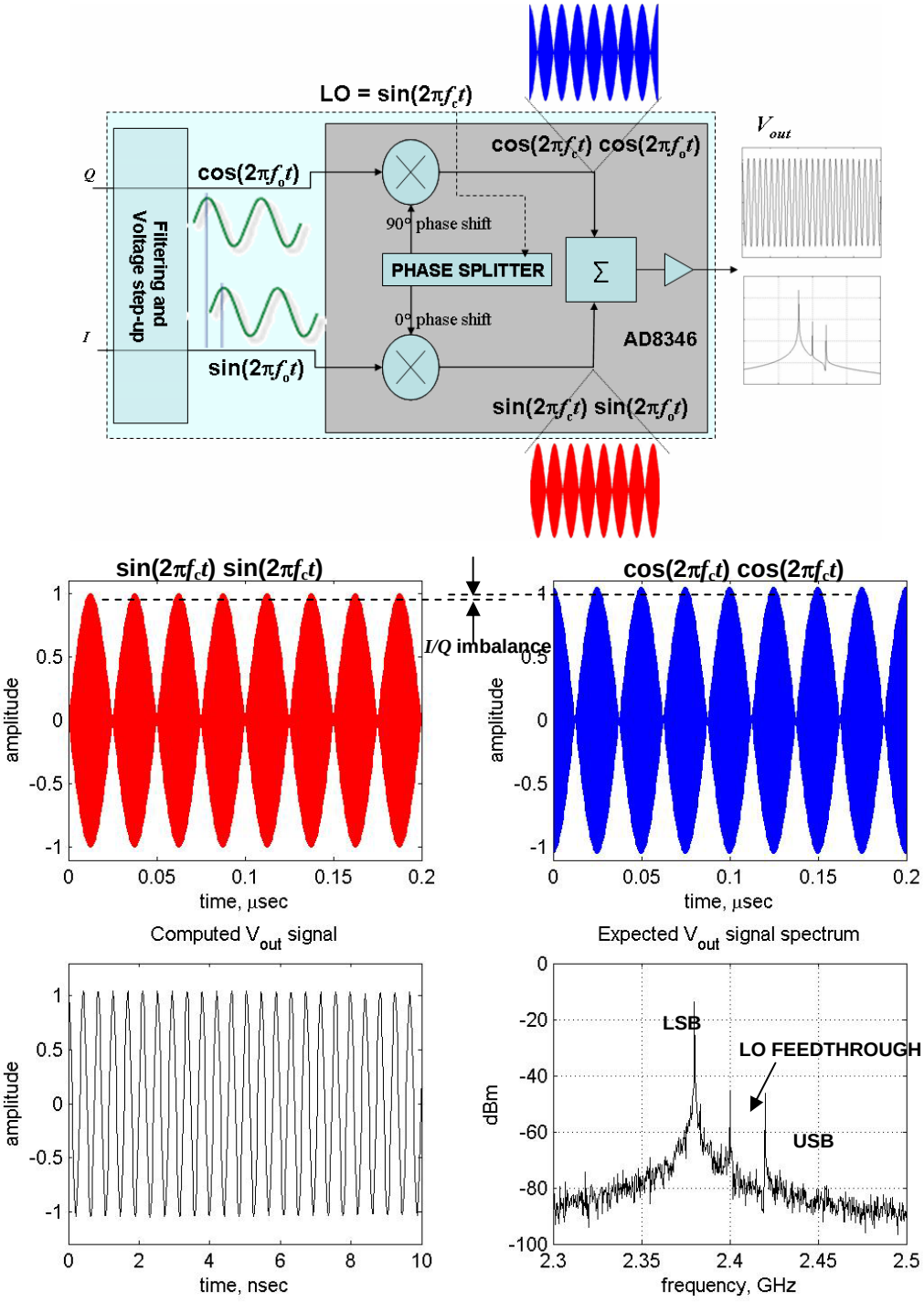


Figure 21. Computed *I/Q* signal and output spectrum for f_o = 20 MHz.

Now let the LO frequency (f_c) to be set at 2.4 GHz and the DDS operating frequency (f_o) chirped from 10 MHz to 120 MHz. Figure 22 shows the results of the calculation. It seems that the reported 36 dBc suppression is also achievable for wideband as well as LFM signals.

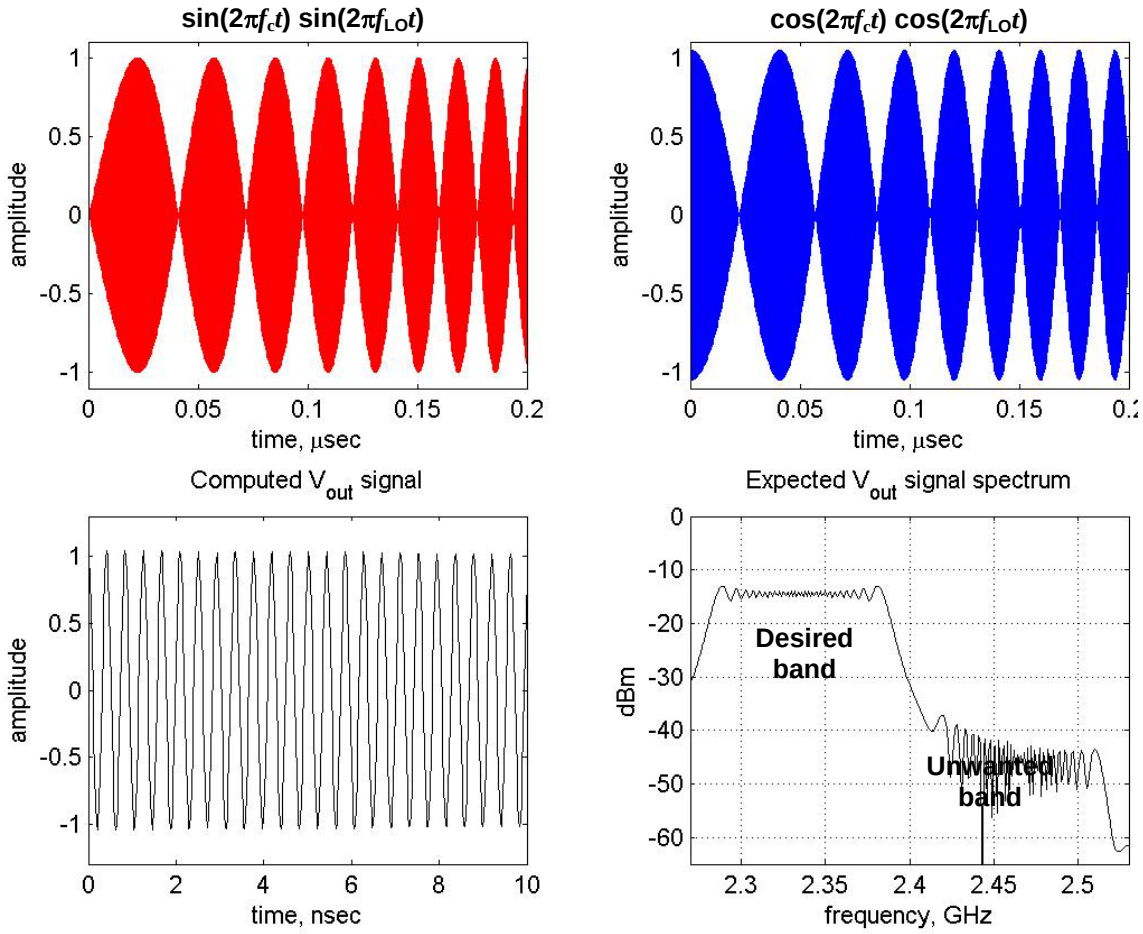


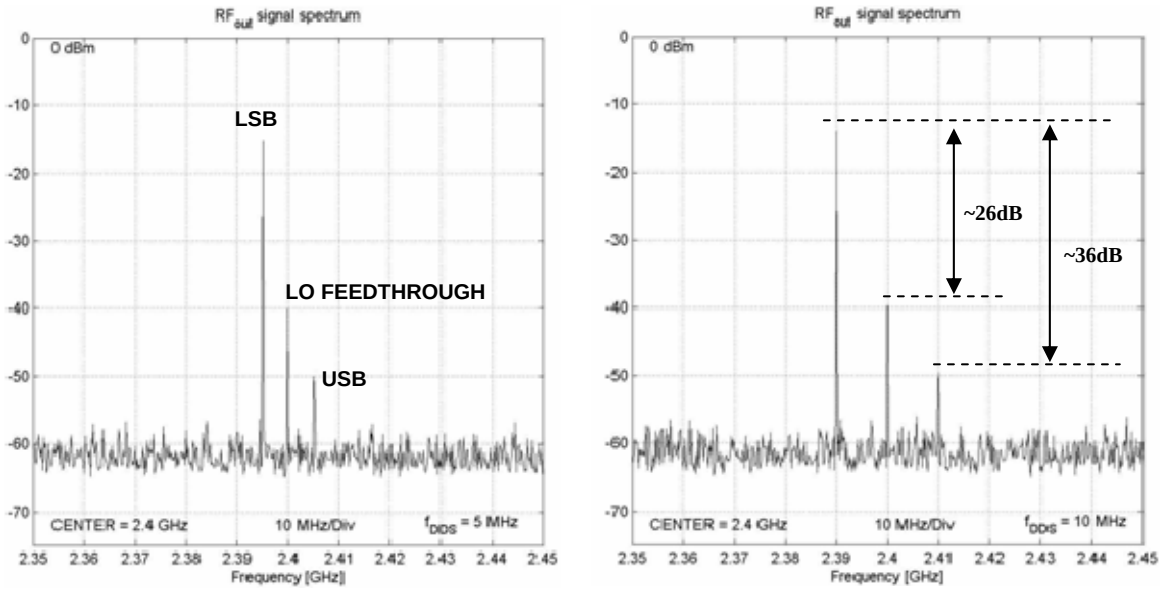
Figure 22. Computed *I/Q* signal and output spectrum for 10 MHz – 120 MHz wideband LFM signal.

2. Experiment Results

The next step is to construct the proposed setup for the laboratory test. For the experiment, the AD9854EVAL evaluation software (revision 1.72) graphic user interface (GUI) was used with the DDS for generating the signals. Chirp mode was selected from the top of the screen and the start frequency (Frequency Tuning Word #1) was set to 1 MHz. Next, the frequency step resolution, 0.01 MHz, is programmed into the 48-bit,

two's complement Frequency Step Word. The external clock input was fed with a 75 MHz frequency sinewave and the DDS's clock multiplier was enabled to x4, hence generating an internal clock rate of 300 MHz. The amplitude was set to full amplitude. The AD8346EVAL board was fed with a 2.4 GHz LO sinewave frequency

On the spectrum analyzer, it was observed that as the DDS frequency slowly chirps from 1 MHz to 20 MHz, the opposing sideband suppression lingers around -36 dBc. Figure 23 shows the image as observed on the spectrum analyzer at DDS frequencies of 5 MHz and 10 MHz respectively.

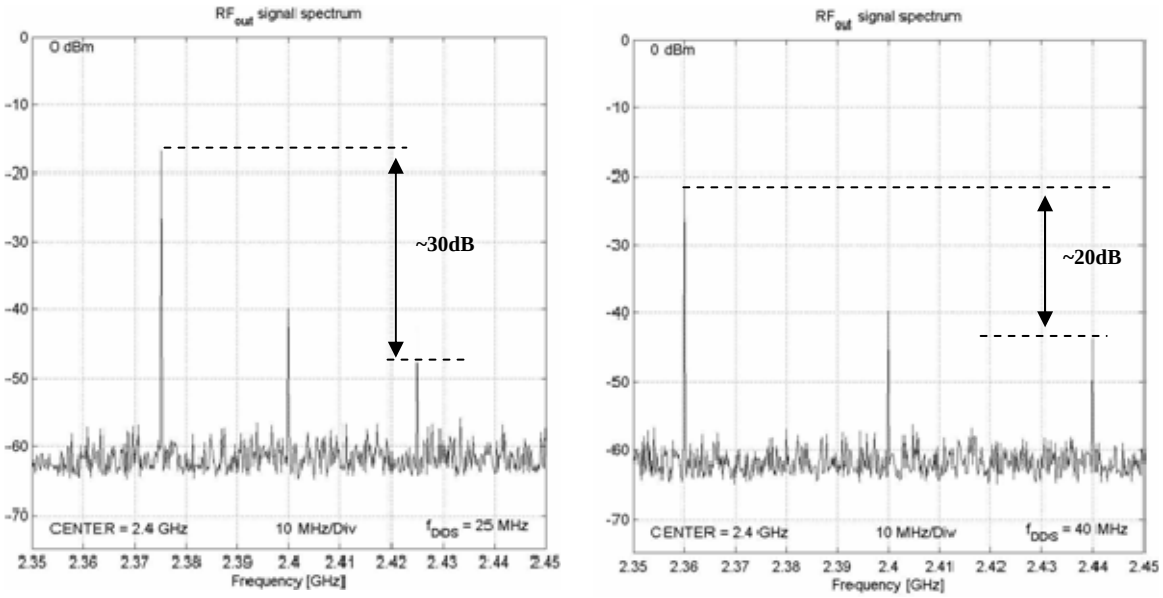


(a) 5 MHz operating frequency. (b) 10 MHz operating frequency.

Figure 23. Spectrum analyzer laboratory results from the upconversion.

The output spectrum remains roughly the same with approximately 36 dBc sideband suppression. However as the operating frequency is increased above 25 MHz, the desired signal strength starts to decrease and the magnitude of the unwanted sideband also increases (but only slightly). The output spectra for operating frequencies of 25 MHz and 40 MHz are shown in Figure 24. The results show a reduction in the suppression level to about ~30 dB and ~20 dB respectively. The suppression level will further decrease with increasing operating frequency and at around 65 MHz, the suppression will

reduce to a mere 10 dB before it drops off as the DDS sweep towards its cutoff frequency (or maximum operating frequency) of 120 MHz.

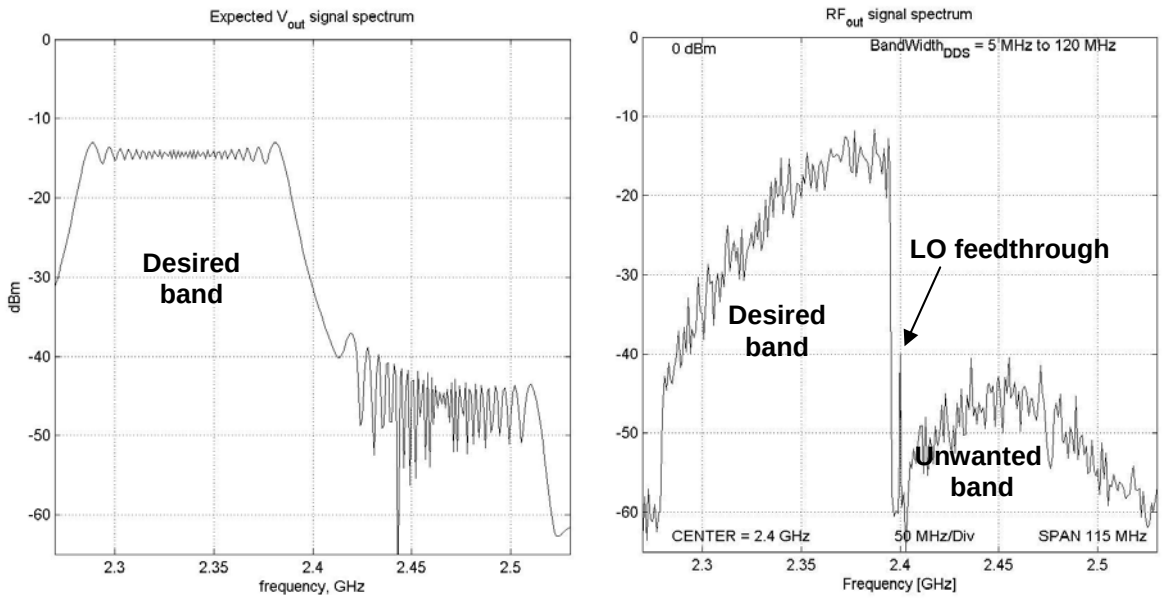


(a) 25 MHz operating frequency.

(b) 40 MHz operating frequency.

Figure 24. Beyond 25 MHz operating frequency the sideband suppression starts to reduce.

The results show that good signal integrity was preserved on the LSB. At some instances (at lower operating frequencies < 10 MHz), signal-to-sideband suppression could be as great as 40 dB. The 40-dB differential equates to a power ratio of about ten-thousand to one. However the available bandwidth with –36 dB suppression seems to be much narrower than computed. The theoretical available bandwidth should be the range at which the DDS can operate (i.e. 120 MHz) as shown in Figure 25(a). The measured bandwidth as shown in Figure 25(b), shows tapering effect as the operating frequency sweeps toward 120 MHz. This results in a lesser suppression level between the desired signal and the unwanted sideband. This is due mainly to the characteristic of the DDS.



(a) Computed 10 – 120 MHz bandwidth. (b) Measured bandwidth.

Figure 25. Instantaneous bandwidth.

The amplitude of the DDS output spectrum are contained in a sinc (or $\sin[x]/x$) envelope which is a result of the zero-order-hold associated with the output circuit of the DDS (typically a DAC). This sinc function inherent in the DAC causes amplitude variations at the DDS output as a function of frequency, this is especially noticeable for wide bandwidth signals as captured in Figure 25(b).

In addition, since fundamentally a DDS is a sampled system, the output spectrum of a DDS system contains the operating frequency (f_o) and its alias frequencies that stretch to infinity. Hence, the output is usually filtered with a low pass filter (LPF) which, in the case of AD9854, has a cutoff frequency (f_{cutoff}) of 120 MHz. This causes the signal to attenuate more steeply as it approaches the cutoff frequency.

Table 1 states the specification for the DAC dynamic output characteristic of the AD9854. What it shows is that for wideband applications, the further the signal is away from baseband, the lower the achievable dynamic range.

DAC DYNAMIC OUTPUT CHARACTERISTICS		
DAC Wideband SFDR	**AD9854ASQ**	**Units**
1 MHz to 20 MHz A_{OUT}	58	dBc
20 MHz to 40 MHz A_{OUT}	56	dBc
40 MHz to 60 MHz A_{OUT}	52	dBc
60 MHz to 80 MHz A_{OUT}	48	dBc
80 MHz to 100 MHz A_{OUT}	48	dBc
100 MHz to 120 MHz A_{OUT}	48	dBc
DAC Narrowband SFDR		
10 MHz AOUT (±1 MHz)	83	dBc
10 MHz AOUT (±250 kHz)	83	dBc
10 MHz AOUT (±50 kHz)	91	dBc
41 MHz AOUT (±1 MHz)	82	dBc
41 MHz AOUT (±250 kHz)	84	dBc
41 MHz AOUT (±50 kHz)	89	dBc
119 MHz AOUT (±1 MHz)	71	dBc
119 MHz AOUT (±250 kHz)	77	dBc
119 MHz AOUT (±50 kHz)	83	dBc

Table 1. AD9854 DAC dynamic output characteristics. (After Ref. [7].)

3. Summary and Comments on Results

a. Limited Bandwidth

Much care had to be taken when trying to achieve the manufacturer's specification with the experiment. The results were consistent with 36 dBc suppression from dc up to 25 MHz before starting to slowly decrease somewhat linearly prior to the complete drop off at 120 MHz.

To maintain a high power ratio between the desired signal and unwanted sideband it might be necessary to limit the DDS operating bandwidth to about 25 MHz. For wider bandwidth application it maybe possible to use the latest AD9959 DDS which has an output frequency up to 200 MHz, instead of 120 MHz in the case of AD9854. The

higher output frequency should provide additional useable bandwidth while maintaining the high power ratio.

b. Comments on the Upconversion

Achieving the performance specified by the manufacturer has been difficult because the setup is very sensitive to phase changes. The initial attempt yielded only a 4-10 dB of suppression, which was later found to be due to the make-shift transformer board and its loose connectors. New boards were re-constructed using new transformers and better quality connectors.

The new boards provided better results with sideband suppression up to –36 dBc as reported in the manufacturer's specification [1]. Although, it was found that the value fluctuates significantly with the sweep operating frequency. The –36 dBc was achievable only at about 10 - 11 MHz operating frequency. Beyond that, the suppression reduced significantly.

The cables used for connecting the transformer to the modulator board in the experiment were of the same length, and hence should not have introduced a significant phase error. Nonetheless they were replaced with new semirigid cables that were phase trimmed. With the new calibrated cables and the new transformer board, the results were more consistent and were able to provide the –36 dBc from 1 MHz up to 25 MHz before decreasing somewhat linearly to –10 dB at around 70 MHz.

As shown in Figure 23 the –36 dBc suppression is achieved more consistently using calibrated cables and properly constructed transformer boards. This contradicts the finding in [5]. Only 4-10 dB suppression was observed using make-shift transformer board and uncalibrated cables. The most probable cause of the finding in [5] could be due to the inadequacy of the transformer circuitry and the low quality cables used in the experiment.

c. LO Leakage

LO feedthrough amplitude (–26 dBc) is greater than the suppressed sideband in this setup. The LO feedthrough level is not affected by either the phase or amplitude of the DDS *I* and *Q* input signals.

LO feedthrough is reduced using active offset nulling techniques. This necessitates a dc-coupled connection between the DAC and modulator. The offset nulling can occur in the digital backend, or the output of the DAC. If done in the digital backend, an additional data processing step is required that might not be convenient and directly reduces dynamic range of the data unless resolution is increased. Alternatively, adding a small DC offset to the DAC output signal, prior to the quadrature modulator will compensate for the channel offsets and reduce the LO feedthrough. Typically at ambient temperature, LO leakage can be held below about –50 dBm over temperature on a modulator which generates a maximum output power of around 0 dBm. Whether this can be achieved with the AD8346 would have to be further investigated.

It is important to note that since the LO feedthrough results from dc offset errors, nulling of LO leakage is independent of frequency to a first approximation. However as frequency increases, LO leakage that results from other internal parasitic circuit elements increases. Offset compensation will still reduce the overall feedthrough, but the nulling will now become more frequency dependent.

B. FULFILLING THE PULSE RADAR REQUIREMENT

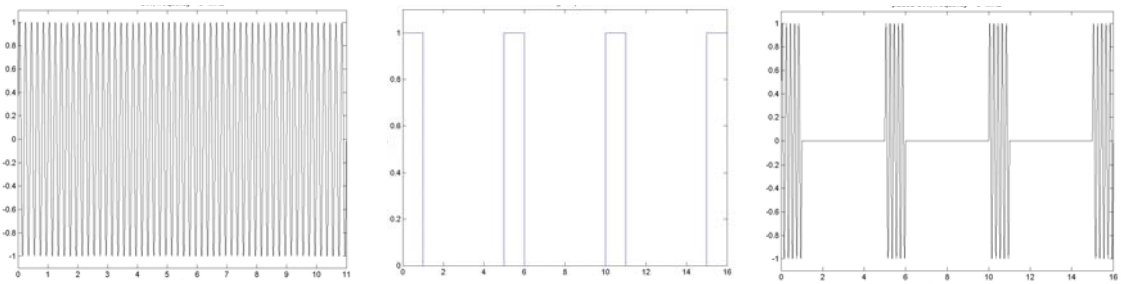
1. Method of Generating Radar Pulses

The RF pulses from the T/R module as shown in Figure 6 and Figure 8 are generated by simply turning on and off the output transmitted signal at the pulse repetition frequency (PRF), f_p. The pulse period is $T_p = 1/f_p$ and the duty cycle τ/T_p. From Fourier theory, the spectrum of a RF signal at frequency f_c that is turned on and off abruptly is similar to the spectrum of a rectangular pulse train displaced in frequency by f_c. Figure 26(c) shows the transmitted pulses obtained by multiplying the CW signal [Figure 26(a)] with a train of pulses [Figure 26(b)]. This relationship can also be expressed mathematically as

$$s(t) = A(t)\cos[\omega_c t + \varphi(t)]) \tag{12}$$

where

$A(t)$ is defined as the rectangular pulse train



(a) Signal [$\cos(\omega_c t)$]. (b) Rectangular wave [$A(t)$]. (c) Output pulses [$s(t)$].

Figure 26. Transmitted pulses generated from switching a RF carrier with a train of rectangular pulses.

2. Matlab Calculation on the Output Pulse Spectrum

Applying the above Fourier theory in Matlab, the output pulse spectrum for the architecture proposed in Figure 8 was calculated. The CW waveform generated by the DDS and the up-converted to 2.4 GHz is put through a pulse switching mechanism. The output spectrum of a train of 5 pulses ($m = 5$) of width $\tau = 500$ ns and a duty cycle of 20% was obtained by finding the Fast Fourier transform of the signal component. Figure 27 shows the output spectrum of the CW versus the pulsed CW.

The Matlab code for generating the waveform can be found in APPENDIX A. The Matlab graphs presented in Figure 28 show the impact on the pulse train spectrum as the pulse width is varied. The operating frequency of the DDS is fixed at 11 MHz and the LO frequency is 2.4 GHz.

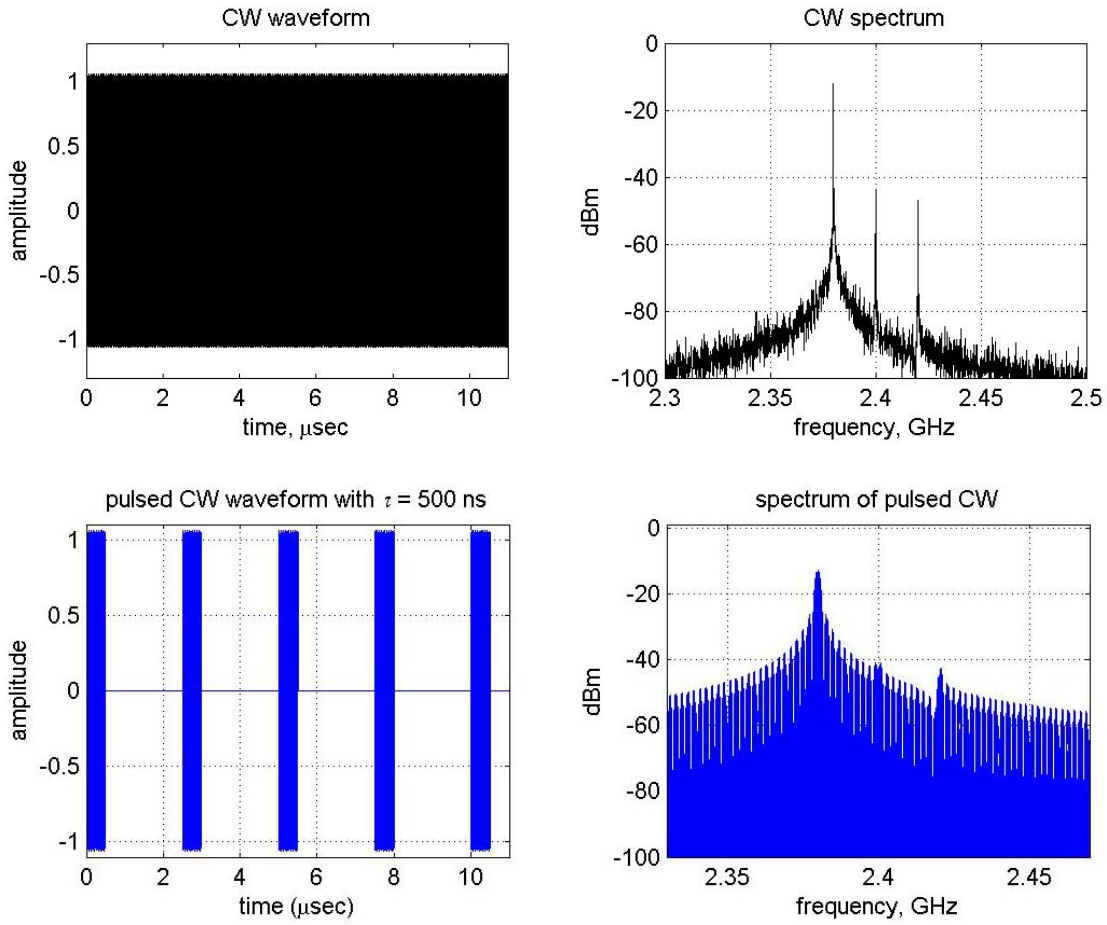
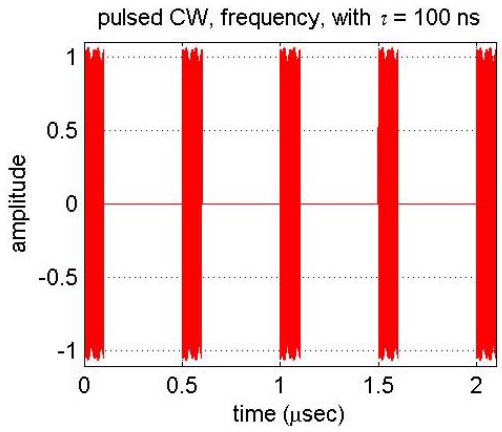


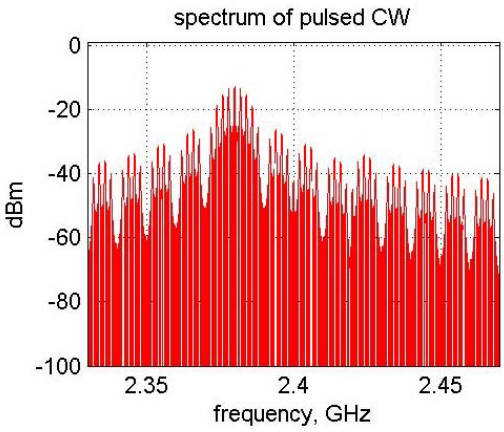
Figure 27. CW (top) and pulsed (bottom) waveforms and spectra at the output of AD8346.

3. Summary and Comments on Pulse Spectrum

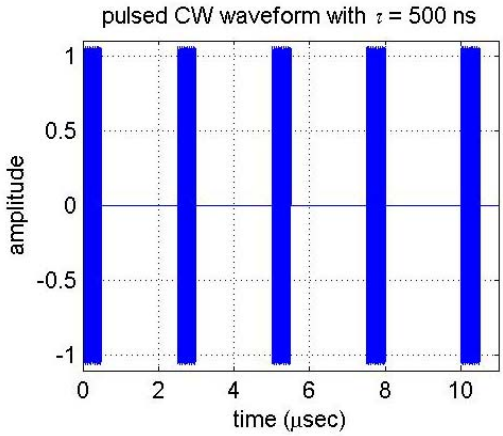
Figure 28(a) and (b) show the signal spectrum for a train of 5 pulses of width 100 ns and a 20% duty cycle. Figure 28 (c) and (d) show the spectrum of a larger pulse of width 500 ns pulse and 20% duty cycle. The general idea here is that for shorter pulses the signal spectrum is generally broader than for longer pulses, and for longer pulses since the spectrum is narrower, it would therefore have lesser power requirement.



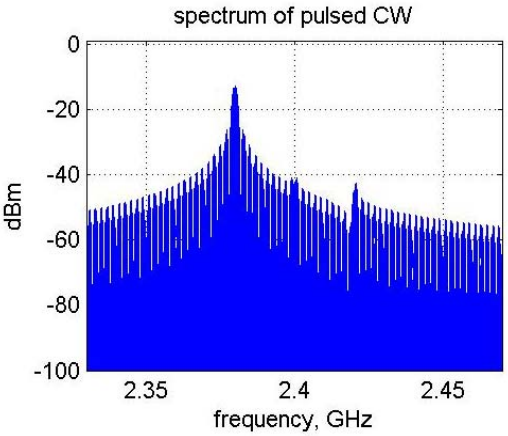
(a) 100 ns pulses with 20% duty cycle.



(b) Signal Spectrum for 100 ns pulses.



(c) 500 ns pulses with 20% duty cycle.



(d) Signal Spectrum for 500 ns pulses.

Figure 28. Signal pulse spectrum for various pulse width.

The equation for determining maximum unambiguous range for a typical pulsed radar is given as

$$R_{\max} = \frac{c}{2 \times PRF} \tag{13}$$

and the equation for determining down range resolution for a particular pulse width is given as

$$\Delta R = \frac{c\tau}{2} \tag{14}$$

where τ is the pulse width.

For an application such as a short range surveillance radar, which requires a detection around 100 km, the pulse width could be around 500 ns to achieve down range resolution of 150 m and pulse repetition frequency of 1 kHz for a typical 150 km maximum unambiguous detection range.

For ballistic missile defense (BMD) which requires detection ranges out to 1000 km and beyond, the required PRF would be much less than 1 kHz, usually around 100 Hz or so to allow a longer pulse width and enough energy on the target thousands of kilometers away so that detection could occur.

C. SYNCHRONIZING MULTIPLE DDS

This section explores the available means of synchronizing multiple DDSs and discusses the best means for use in the construction of the 2.4 GHz radar.

Currently there are primarily two means of synchronizing multiple DDSs. The most common is the existing means of synchronizing the AD9854 DDS, which has been described by *Analog Devices* in their application note [10]. A newer method is used by the AD9958/59 from *Analog Devices,* which has built in synchronization function to connect and automatically synchronize multiple AD9958/59 DDSs.

The following is a brief description on the method proposed in reference [10] on how to synchronize two or more of AD9852/54 based devices.

1. Synchronizing Multiple AD9852/54 DDS-Based Synthesizers

The first requirement for successful synchronization of multiple AD9852/AD9854s is that there must be minimal phase error between the REFCLK inputs to all DDSs. Any difference in phase between the REFCLK edges will result in a proportional phase difference at the DDS outputs. Therefore, careful clock distributions must be maintained in the layout of the PCB as in Figure 19.

Once a fast-edged and properly routed REFCLK signal is provided, the next timing requirement is the coincident transfer of the data into the DDS programming registers. The I/O UPDATE CLK transfers the contents of the I/O port buffer to the

programming registers where data becomes active. Synchronization of multiple DDSs requires that the EXT I/O UPDATE CLK's rising edge occur simultaneously at all DDSs, just like the REFCLK. In addition, the rising edge of the EXT I/O UPDATE CLK must occur at the proper time with respect to REFCLK.

Figure 29 presents one possible reference signal distribution design for the successful synchronization of multiple DDSs. This example shows how to place two DDSs into the same phase relationship.

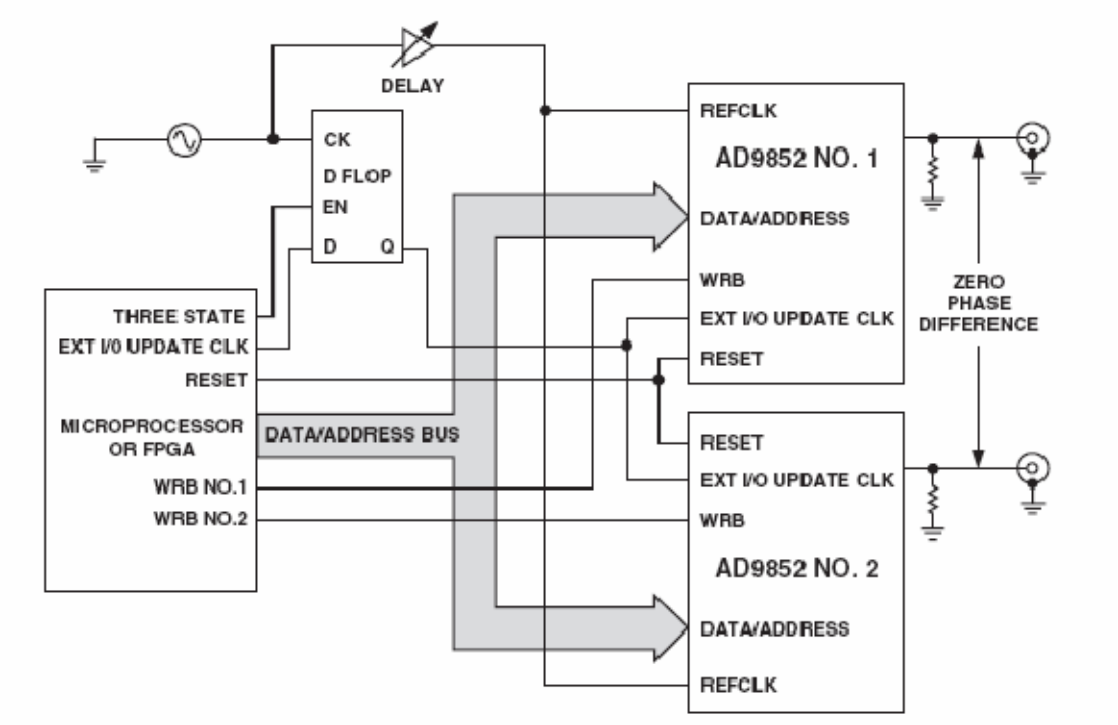


Figure 29. Application Circuit. (From Ref. [10].)

In Figure 29, the D flip-flop enables the EXT I/O UPDATE CLK to be synchronous with the REFCLK and provides a setup time. Proper operation may require additional time delay in the REFCLK path. This delay depends on the CK–to–Q propagation time of the flip-flop.

With proper care and operation, synchronization can be achieved among multiple DDSs.

2. Synchronizing Multiple AD9958/59 DDS-Based Synthesizers

This section explores the second possible method of synchronizing multiple DDS using the latest DDS technology from *Analog Devices*. Released only recently, the AD9958/59 is designed to alleviate the design complexities typically involved in the synchronization of multiple DDS devices. The independent channels of the AD9959 and AD9958 are internally synchronized by a common reference clock. Programmable channel control allows for correction of imbalances in external signal paths due to analog processing, such as filtering, amplification, or PCB layout mismatches. If additional channels are required, the AD9959 and AD9958 allow daisy chaining of additional DDS chips. Reference [11] provides some insights to this automatic synchronizing feature and is briefly described in the following paragraphs.

The AD9959 allows easy synchronization of multiple AD9959 devices. At power-up, the phase of SYNC_CLK can be offset between multiple devices. To correct for the offset and align the SYNC_CLK edges, there are three methods (one automatic mode and two manual modes) of synchronizing SYNC_CLKs. These modes force the internal state machines of multiple devices to a known state, which aligns SYNC_CLKs. Any mismatch in REF_CLK phase between devices results in a corresponding phase mismatch on the SYNC_CLKs.

The various DDS devices are configured as master and slaves, depending on their respective roles. Multiple-part synchronization can be achieved by a simple connection of the SYNC_OUT pin on the master device to the SYNC_IN input of the slave devices.

In Figure 30, the sync pulse is sent from the master to the "Synchronization Delay Equalization" circuitry outside the AD9959/58 chip. The goal is to simultaneously distribute this pulse to the SYNC_IN pins of the slave devices. The slave devices sample the synchronization pulse from the master and compare the clock-generation, state-machine current state against an "expected" value. If the slave device's clock-generation state machine compares properly with that value, the devices are synchronized. If the slave device's clock-generation state machine and the expected value are not identical, the device stalls the clock-generation state machine for one system-clock cycle. This procedure synchronizes the slave device(s) within three SYNC_CLK periods.

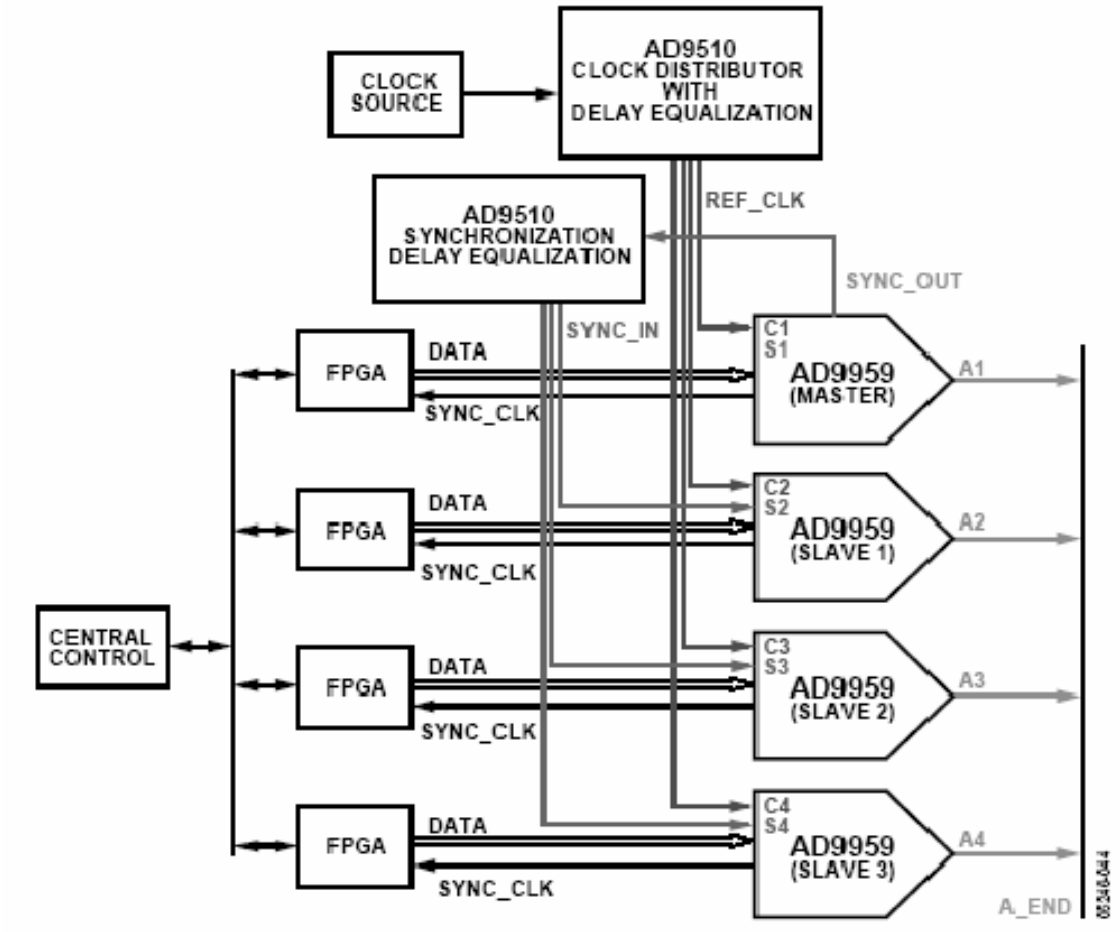


Figure 30. Typical configuration for synchronizing multiple AD9959/58 devices. (From Ref. [11].).

3. Wireless Synchronization of Multiple DDSs

In principle both synchronization techniques can be implemented in a wireless domain. The complexity offered in method 1 requires precise fabrication of the clock distribution circuit and accurate calibration of all paths. In terms of a wireless implementation effort, it would be significant since it requires knowledge of the propagation paths and the precise phase delay that exists from one T/R module to the next. Synchronization may be achieved by carefully measuring the propagation delays and implementing appropriate delay circuitry in each individual T/R module to compensate for these phase delays. This sounds reasonable if synchronization is only for a handful of devices, but for the opportunistic array, it may not be practical as the potential number of T/R modules range into the thousands.

In comparison, the second method uses SYNC pulse generated by a master device and distributed to a cluster of slave devices. Individual slave devices will compare their SYNC pulse to the master's SYNC pulse and determine how much out-of-sync they are with the master and account for the phase differences that exist. Generally synchronization can be achieved within three SYNC pulses with this technique and it is extremely simple and effective even in a wireless domain.

Section B.3 of Chapter IV recommends a method of using this synchronization technique to also synchronize the LO signal which is required for the AD8346 modulator and AD8347 demodulator.

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IV. CONCLUSION AND RECOMMENDATION

O divine art of subtlety and secrecy! Through you we learn to be invisible, through you inaudible and hence we can hold the enemy's fate in our hands.

Sun Tzu

A. CONCLUSION

1. Summary

Radar systems play an important role in modern military tactics and strategy. The radar system of today provides the high value picture to our forces, on which the commander relies for planning its every move. It however also provides the enemy commander valuable information on the movements of these spying units, simply because of the big and unstealthy antenna design that broadcast to the world of its own whereabouts.

As technology continues to evolve, more complex radar designs and techniques will become available. The radar system of tomorrow will not be a system that simply detects targets; it will be to achieve the effect of "to see and not be seen". As the famous military strategist *Sun Tzu* brings out; being invisible and inaudible, we hold the enemy's fate in our hands. By providing the ability to fuse into a stealthy ship without altering its stealth characteristic, the Aperstructure concept provides the solution to achieving this effect.

The key to realizing the opportunistic aperstructure radar concept is to achieve the ability to perform the operations of self-synchronize, synthesize, modulate and demodulate radar waveforms all in one module without any physical connections to the main radar controller. Of these operations the concepts for synchronization and radio frequency (RF) synthesis were explored in this thesis.

2. Results and Discussion

At present COTS DDS can only synthesize signals up to the frequency of 400 MHz. For this reason DDS is routinely being incorporated with a phase-locked loop

(PLL) or up-converted with a mixer. In re-verifying the findings in [5], which concluded that the upconversion technique would not provide the 36 dBc image suppression, it was found that the conclusion arose from inadequate hardware. Using better quality boards and connectors, the laboratory results consistently showed that the 36 dBc was indeed achievable. Below 25MHz the high power ratio between the carrier and the image signal relaxes the filtering requirement and hence reduces the complexity of the transmit module design.

Also, the methods of generating FMCW waveforms and pulsed waveforms from the digital transmit module were investigated. By itself, the DDS is capable of synthesizing various types of waveforms including FMCW. However to generate a pulsed waveform, there is a need to modify the setup to the architecture as proposed in Figure 8. The proposed setup is able to provide coherent pulsed waveforms that are beneficial for many radar applications.

Subsequent investigation was centered on exploring the potential means of synchronizing multiple DDSs. This is a requirement for synchronizing the potentially hundreds of elements of the array that could cover the entire surface of a large ship. The existing means of synchronizing the AD9854 model of DDSs involves a delicate process of distributing the REFCLK signal to each individual DDS without incurring any phase differences between them. This is generally achievable if the number of DDSs to be synchronized does not become too large. However, for our application, the potential number of DDS that needs to be synchronized range into the hundreds and hence would be impractical if not unfeasible to implement. Fortunately *Analog Devices* has recently released a new range of DDS (AD9958-AD9959) that has built-in self-synchronization feature. This new method of synchronization provides the ability to connect these DDSs in a daisy chain that allows for large numbers of DDS to be synchronized.

B. RECOMMENDATION

1. Exploiting New Technologies

With the new range of DDSs that has just been released by *Analog Devices*, it is prudent to explore their new capabilities and ascertain if they could be utilized in our

application. The following two new features in the latest range of DDS (AD9958-AD9959) from *Analog Devices* are worth considering for further investigation.

2. Improved Bandwidth

Unlike AD9854 that synthesizes RF frequencies only up to 120 MHz, the newer range of DDSs (AD9958-59) can synthesize frequency up to 200 MHz. The extra frequency range could theoretically provide additional bandwidth that may be helpful for many wideband applications. As tested, although the AD9854 can synthesize up to 120 MHz, it could only provide up to 25 MHz bandwidth if a high power ratio were to be maintained. With the 200 MHz AD9958-59, this bandwidth could be extended, which should accommodate larger bandwidth applications.

Lab results from the manufacturer [12] have shown that the AD9959/58 device enables better than –60 dBc suppression of the redundant sideband. Figure 31 show the results of a 25 MHz, single tone that is upconverted to 975 MHz using quadrature signals from the AD9959.

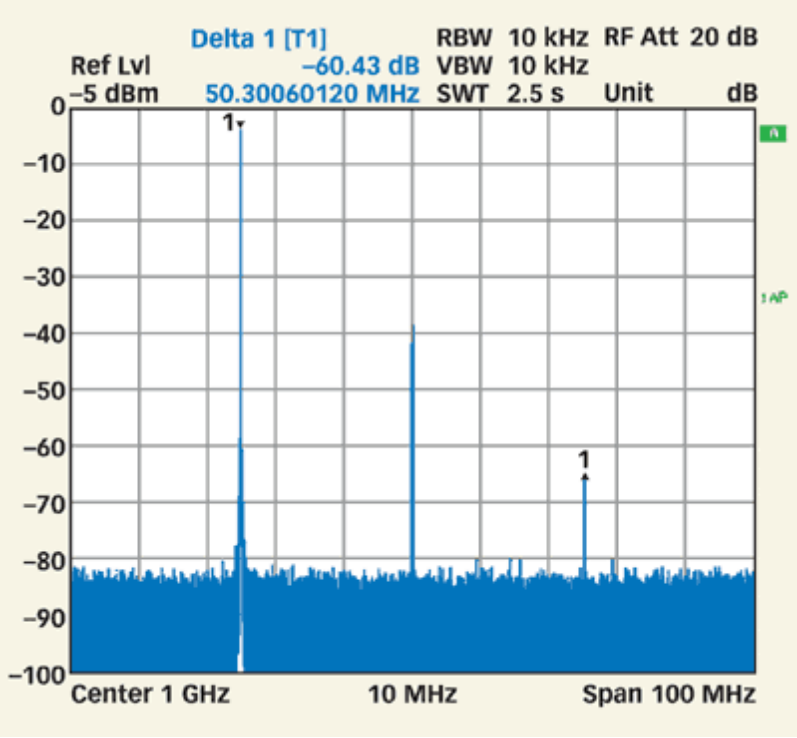

Figure 31. 25 MHz, single tone being upconverted to 975 MHz using quadrature modulation. (From [12].)

3. Wireless Synchronization of Multiple T/R Modules

One of the most significant improvements of AD9959/58 over previous generations is the introduction of a multiple device synchronization feature. This new feature should be further explored as it provides a promising means not only to synchronize the multiple DDS devices but also applicable to synchronizing the LO signal which is required for the AD8346 modulator and AD8347 demodulator.

The distribution of the LO (required by the modulator and demodulator) and the REFCLK (required for the DDS) signals can be combined into a single waveform. A pulse train could be transmitted from the centralized controller and the pulse train envelope detected and used for timing. The carrier can be extracted and used for the LO. Hardware for performing the synchronization must be included in each T/R module. The "beam tagging" method [14] has shown the capability to phase synchronize large number of elements.

A combination of wired and wireless techniques could be applied to the opportunistic array. For example a cluster of elements can be slaved to neighboring "masters" by hardwired paths. The centralized controller would then only have to synchronize a smaller number of masters.

4. Proposed Modification

The latest AD9959 provides four independent channels, which theoretically should be configurable to support different applications simultaneously. This feature can eliminate the need for more synchronization that will be required for the pulse switching and generating mechanism. It might be worthwhile exploring the remaining DDS channels to drive the pulsing requirement. Since all channels are inherently synchronized because they share a common system clock, which effectively eliminates the need to synchronize multiple devices. With a single-chip solution, the temperature effects that exist between two separate devices are essentially eliminated as well.

Figure 32 illustrates how an AD9959 can be hooked up to drive the pulsing requirement. However it should be noted that the rectangular wave generated by the AD9959 DDS to drive the pulse switching mechanism may not meet all pulse radar

requirements. Further investigation into the proposed setup would be necessary to determine the range of PRFs it can support and the speed at which the DDS can change the PRF frequency.

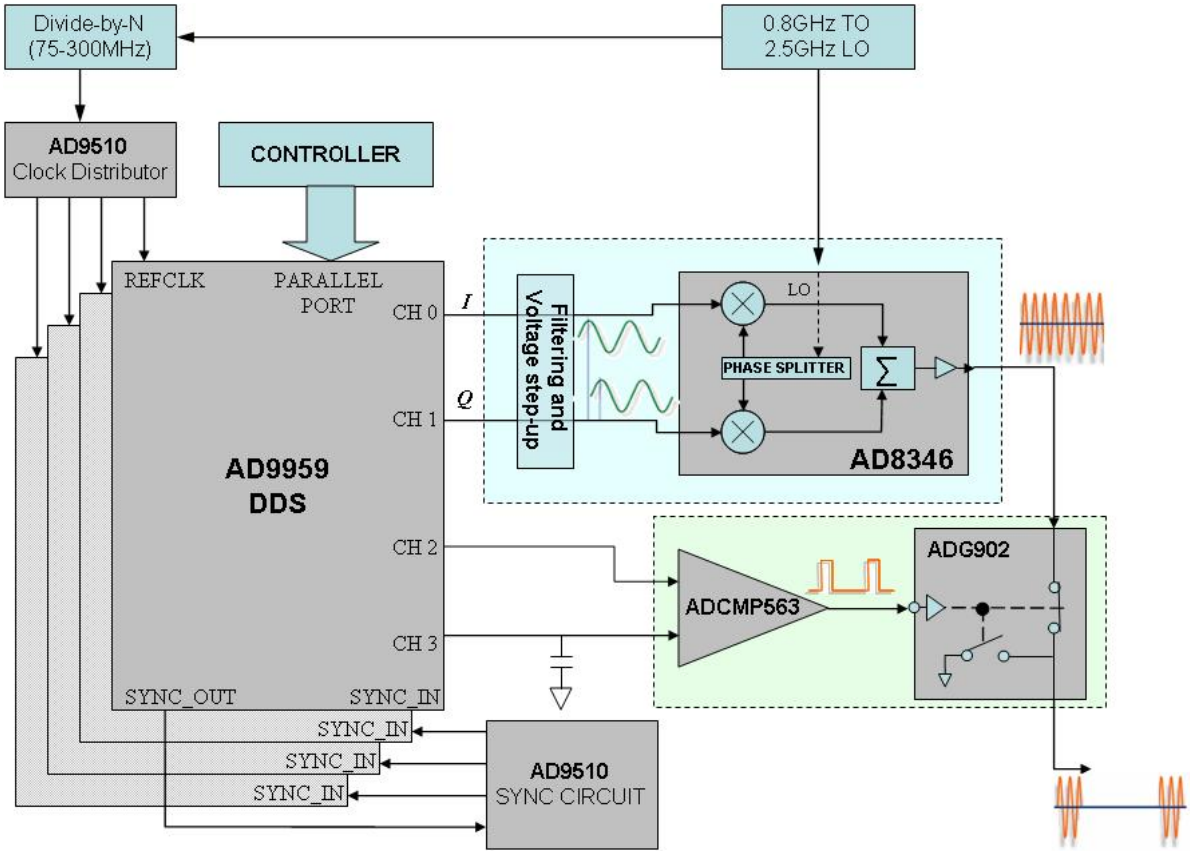

Figure 32. Proposed circuit for generating a pulse train using the AD9959 DDS.

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APPENDIX A. MATLAB SIMULATION PROGRAMS

This appendix contains several matlab programs that computes the expected signals and spectra for the upconversion experiments at various stages.

```
%=====================================================================
% This matlab program computes the I and Q signal as well as the output
% spectrum from the AD9854 + AD8346 upconversion setup.

clf
clear
DDS_fmhz = 20;          % (MHz) DDS operating frequency
LO_fghz = 2.4;          % (GHz) Local Oscillator frequency
phi=deg2rad(1);         % Introduce a 1 degree phase error between I&Q signal
aif=1.00;               % amplitude of I signal from DDS
aqf=10^(0.2/10);        % amplitude of Q signal with a 0.2 dB imbalance compare to I signal
V_OSBB=10^(-29/20);     % Introduce a -29 dBc LO feedthrough offset voltage

f_LO = LO_fghz*1e9;
f_DDS = DDS_fmhz*1e6;
w_DDS = 2.*pi.*f_DDS; % convert frequency to omega radian
w_LO = 2.*pi.*f_LO;     % convert frequency to omega radian
t = 0:1/(20*f_LO):3e-6;  % time

Isignal=aif.*sin(w_DDS*t).*sin(w_LO*t);          % compute I x LO(sine)signal
Qsignal=aqf.*cos(w_DDS*t+phi).*cos(w_LO*t);      % compute Q x LO(cosine)signal with phase
                                                 % error of phi
LO_leakage=V_OSBB.*sin(w_LO.*t);                 % simulated LO_feedthrough

Vout=Isignal+Qsignal+LO_leakage;                 % Vout with LO feedthrough
VoutSpec=fft(Vout,length(Vout));                 % FFT spectrum Vout
Voutnorm=abs(VoutSpec)/max(abs(VoutSpec)); % normalised FFT spectrum
PoutdBm=20.*log10(Voutnorm);                     % Convert to dBm scale
P_dBm = PoutdBm-13%[dBm];                        % Scale output peak to the max o/p power from
                                                 % AD8346 which is spec at -13 dBm
RFout = awgn(P_dBm,-10);                         % add white gaussian noise

% Convert time scale to frequency scale
delf=1/max(t);
Nf=length(VoutSpec)-1;
f=[0:Nf]*delf;

% Plot figures
figure(1),subplot(221);                  % plot I signal vs time
plot(t/1e-6,Isignal,'r'),xlabel('time, \musec'),ylabel('amplitude') ;
title('Computed \it{I} signal'),axis([0,0.2,-1.1,1.1]);

figure(1),subplot(222);                  % plot Q signal vs time
plot(t/1e-6,Qsignal,'b'),xlabel('time, \musec'),ylabel('amplitude') ;
title('Computed \it{Q} signal'),axis([0,0.2,-1.1,1.1]);

figure(1),subplot(223);                  % plot Vout vs time
plot(t/1e-9,Vout,'k'),xlabel('time, nsec'),ylabel('amplitude') ;
```

```
title('Computed V_o_u_t signal'),axis([0,10,-1.3,1.3]);

figure(1),subplot(224);                    % plot Vout signal spectrum with dBm scale
plot(f/1e9,RFout,'k');axis([LO_fghz-0.1,LO_fghz+0.1,-100,0]);grid on;
xlabel('frequency, GHz'),ylabel('dBm')
title('Expected V_o_u_t signal spectrum');

figure(2);
plot(f/1e9,RFout,'k');axis([LO_fghz-0.1,LO_fghz+0.1,-100,0]);grid on;hold on;
image(RFout);colormap bone;
xlabel('frequency, GHz'),ylabel('dBm');
title('Expected V_o_u_t signal spectrum');

%=========================================================================


%=========================================================================
% This matlab program repeats the above, but now the I and Q signal from DDS will be LFM from
10 MHz to 120 MHz.


clf
clear
DDS_fmhz = 50          % (MHz) DDS operating frequency
DDS_0 = 10e6           % (MHz) DDS starting frequency
DDS_F = 120e6;         % (MHz) DDS ending frequency
LO_fghz = 2.4;         % (GHz) Local Oscillator frequency
aif=1.00;              % amplitude of I signal from DDS
aqf=10^(0.2/10);       % amplitude of Q signal from DDS with a 0.2 dB imbalance compare to I
signal
V_OSBB=10^(-29/20);    % Introduce a -42dBm or ~ -29 dBc LO feedthrough offset voltage

f_LO = LO_fghz*1e9;
f_DDS = DDS_fmhz*1e6;
w_DDS = 2.*pi.*f_DDS; % convert frequency to omega radian
w_LO = 2.*pi.*f_LO;    % convert frequency to omega radian
t = 0:1/(20*f_LO):1e-6;  % time

cos_f=chirp(t,DDS_0,1e-6,DDS_F,'linear',0);     % Chirp DDS operating freq from 10MHz to
                                                % 120MHz
sin_f=chirp(t,DDS_0,1e-6,DDS_F,'linear',-91);   % Choose 91 instead of 90 to introduce a 1
                                                % degree phase error

Isignal=aif.*sin_f.*sin(w_LO*t);                % compute I x LO(sine)signal
Qsignal=aqf.*cos_f.*cos(w_LO*t);                % compute Q x LO(cosine)signal with phase
                                                % error of phi
LO_leakage=V_OSBB.*sin(w_LO.*t);                % simulated LO_feedthrough

Vout=Isignal+Qsignal+LO_leakage;                % Vout with LO feedthrough
VoutSpec=fft(Vout,length(Vout));                % FFT spectrum Vout
Voutnorm=abs(VoutSpec)/max(abs(VoutSpec)); % normalised FFT spectrum
PoutdBm=20.*log10(Voutnorm);                    % Convert to dBm scale
P_dBm = PoutdBm-13%[dBm]                        % Scale output peak to the max output power
                                                % from AD8346 which is spec at -13 dBm
```

```
RFout = awgn(P_dBm,-5);                    % add white gaussian noise

% Convert time scale to frequency scale
delf=1/max(t);
Nf=length(VoutSpec/2)-1;
f=[0:Nf]*delf;

% Plot figures
figure(1),subplot(221);                    % plot I signal vs time
plot(t/1e-6,Isignal,'r'),xlabel('time, \musec'),ylabel('amplitude') ;
title('Computed \it{I} signal'),axis([0,0.2,-1.1,1.1]);

figure(1),subplot(222);                    % plot Q signal vs time
plot(t/1e-6,Qsignal,'b'),xlabel('time, \musec'),ylabel('amplitude') ;
title('Computed \it{Q} signal'),axis([0,0.2,-1.1,1.1]);

figure(1),subplot(223);                    % plot Vout vs time
plot(t/1e-9,Vout,'k'),xlabel('time, nsec'),ylabel('amplitude') ;
title('Computed V_o_u_t signal'),axis([0,10,-1.3,1.3]);

figure(1),subplot(224);                    % plot Vout signal spectrum in dBm scale
plot(f/1e9,RFout,'k');axis([LO_fghz-0.15,LO_fghz+0.15,-100,0]);grid on;
xlabel('frequency, GHz'),ylabel('dBm')
title('Expected V_o_u_t signal spectrum');
%=========================================================================




%=========================================================================
% This matlab program computes the I and Q signal as well as the output
% spectrum from the AD9854 + AD8346 upconversion setup.

clf
clear
DDS_fmhz = 20;          % (MHz) DDS operating frequency
LO_fghz = 2.4;          % (GHz) Local Oscillator frequency
phi=deg2rad(1);         % Introduce a 1 degree phase error between I&Q signal
aif=1.00;               % amplitude of I signal from DDS
aqf=10^(0.2/10);        % amplitude of Q signal from DDS with a 0.2 dB imbalance compare to I
signal
V_OSBB=10^(-29/20);   % Introduce a -29 dBc LO feedthrough offset voltage

f_LO = LO_fghz*1e9;
f_DDS = DDS_fmhz*1e6;
w_DDS = 2.*pi.*f_DDS;   % convert frequency to omega radian
w_LO = 2.*pi.*f_LO;       % convert frequency to omega radian

%=========================================================================
% The following section computes the pulse train waveform and its spectrum
%
% compute the power in the transmitted spectrum

Np=5;                   % number of pulse widths in a period (T=Np*tau)
tau=0.5e-6;             % pulse width
```

```
N=5;                        % number of pulses
Nt=4096;                    % number of time samples per pulse width
T=Np*tau;
%_____________________ compute plot the pulsed CW _________________
 dt=tau/Nt;
  it=T/dt;
  k=0; sum=0;
   for n=1:N
    for i=1:it
      k=k+1;
      to=(i-1)*dt;
      t(k)=to+(n-1)*T;
        Isignal=aif.*sin(w_DDS*to).*sin(w_LO*to);          % compute I x LO(sine)signal
        Qsignal=aqf.*cos(w_DDS*to+phi).*cos(w_LO*to);  % compute Q x LO(cosine)signal with
phase error of phi
        LO_leakage=V_OSBB.*sin(w_LO.*to);                  % simulated LO_feedthrough

      S(k)=0;
       if to <= tau
        S(k)=Isignal+Qsignal+LO_leakage;
sum=sum+S(k);
        end
    end
 end
Psig=(sum*dt)^2;  % power in the signal for normalization

%___________________ compute the Fourier transform ___________________
% there are now k time samples; increase it by a factor of NN
% before taking the fft (by zero packing)
NN=4;
S(k+1:NN*k)=zeros(1,(NN-1)*k);
t(1:NN*k)=dt*[0:NN*k-1];
A=fft(S,length(S)); Amax=max(abs(A));
figure(1)
subplot(221)
plot(t/1e-6,S,'b'),xlabel('time (\musec)'),ylabel('amplitude')
title(['pulsed CW, frequency, with {\it\tau} = ',num2str(tau/1e-9),' ns'])
grid,axis([0,max(t)/5e-6+1,-1.1,1.1])
F=fftshift(A);
delf=1/max(t); Fmax=max(abs(F));
Nf=length(F)/2-1;
f=[0:Nf]*delf;      % frequencies
Fp=F(length(F)/2+1:length(F));
Fn=abs(Fp)/Fmax;                                % normalized spectrum
PdBm=20.*log10(Fn)-13;                          % conver to dBm scale
subplot(222)
plot(f/1e9,PdBm,'b');axis([LO_fghz-DDS_fmhz/1e3-0.05,LO_fghz+DDS_fmhz/1e3+0.05,-100,1])
xlabel('frequency, GHz'),ylabel('dBm')
title('spectrum of pulsed CW'); grid on;
```

APPENDIX B. SURVEY ON NEW COMMERCIAL DDS

The key manufacturer and global leader in high performance semiconductors such as direct digital synthesizers (DDS) is Analog Devices Inc. (NYSE: ADI). The company had developed an extensive range of DDS and is continuing to introduce new families of direct digital synthesizers packed with more features and capabilities to meet modern demand and applications.

This survey summarizes the new features and capabilities arising from the development in the direct digital synthesizer that might be useful for future work. The following information are taken or quoted from http://www.analog.com.

Complete DDS solution (AD9852-AD9854)

The AD9854 digital synthesizer is a highly integrated device that uses advanced DDS technology, coupled with (2) internal high-speed, high performance quadrature D/A converters and comparator to form a digitally-programmable I & Q synthesizer function.

When referenced to an accurate clock source, the AD9854 generates a highly stable, frequency, phase and amplitude programmable sine and cosine outputs that can be used as an agile L.O. in communications, radar, and many other applications.

The AD9854's innovative high-speed DDS core provides a 48-bit frequency tuning word, which results in an output tuning resolution of 1 micro-Hertz, for a 300 MHz internal reference clock input. The AD9854's circuit architecture allows the generation of simultaneous quadrature outputs at frequencies up to 150 MHz, which can be digitally tuned at a rate of up to 100 million new frequencies per second. The (externally filtered) sine wave output can be converted to a square wave by the internal comparator for agile clock generator applications. The device provides 14-bits of digitally-controlled phase modulation and single-pin PSK. The on-board 12-bit I & Q DACs, coupled with the innovative DDS architecture, provide excellent wideband and narrowband output SFDR. The Q-DAC can also be configured as a user-programmable control DAC if the quadrature function is not desired. When configured with the onboard comparator, the 12-bit control DAC facilitates pulse-width modulation (PWM) and static

duty cycle control, in the highspeed clock generator application. Two 12-bit digital multipliers permit programmable amplitude modulation, shaped on-off keying and precise amp-litude control of the quadrature outputs. The AD9854's programmable 4^x - 20^x REFCLK Multiplier circuit generates the 300 MHz clock internally from a lower frequency external reference clock. This saves the user the expense and difficulty of implementing a 300 MHz clock source. Direct 300 MHz clocking is also accommodated with either single-ended or differential inputs. Single-pin conventional FSK and the enhanced spectral qualities of "ramped" FSK are supported. The AD9854 uses advanced .35 micron CMOS technology to provide this high level of functionality on a single +3.3 V supply

GigaHertz complete DDS (AD9858) [Sep/2002]

The AD9858 DDS is a flexible device that consists of a power-efficient DDS core, a 32-bit phase accumulator, 14-bit phase offset adjustment, and a 1 GSPS 10-bit DAC. It features an analog mixer capable of operating at 2 GHz, a phase-frequency detector (PDF), and a programmable charge pump (CP) with advanced fast-lock capability. These RF building blocks can be used for various frequency synthesis loops or as needed in system design.

The new DDS can directly generate frequencies up to 400+ MHz when driven at 1 GHz internal clock speed. The reference clock can be derived from an external clock source of up to 2 GHz by using the on-chip divide-by-2 feature. The on-chip mixer and PFD/CP make possible a variety of synthesizer configurations capable of generating frequencies in the 1-2 GHz range or higher.

The AD9858 is easily configured by writing data to its on-chip digital registers that control all operations of the device. In addition, it can be programmed to operate in single-tone mode or in a frequency-sweeping mode. To reduce power consumption, there is also a programmable full-sleep mode.

Low-Power (AD9951-AD9954) [June/2003]

These chips deliver a 400 MHz clock speed at one-tenth the power consumption of previous solutions. This now enables designers to use DDS for fast frequency hopping at higher output frequencies in more power-sensitive applications. Typical applications include satellite communications, broadband networking, radar, test and measurement, and instrumentation.

The AD9954 devices can clock at 400 MSPS and synthesize frequencies of up to 160 MHz while dissipating less than 200 mW of power. Previous DDS chips of comparable resolution could only synthesize frequencies up to 120 MHz and dissipated 2 watts of power. The lower power dissipation now allows designers to use multiple chips on a single PCB with less concern for thermal issues. Additional features of the family include an integrated 14-bit digital-to-analog converter, on-chip random access memory (RAM), phase offset and amplitude control, and multi-chip synchronization.

The new DDS family comprises four new 14-bit devices with various added benefits. The feature sets were selected to allow designers to purchase only the functionality needed for the desired application. The four family members and added functionality are the following:

AD9951: Basic DDS with on-board 14-bit DAC
AD9952: with high-speed comparator
AD9953: with RAM (allows nonlinear phase / frequency sweeping)
AD9954: with high-speed comparator, RAM, and automatic linear frequency sweep

Multi-channel (AD9958 and AD9959) [July/2005]

ADI's new four-channel AD9959 and two-channel AD9958 deliver greater control to correct imbalances between multiple signals. For space-constrained systems, the AD9958 and AD9959 simplify the design process by integrating multiple DDS channels on a single chip, eliminating the need for several single- channel DDS chips and external circuitry and offering dramatic board space reduction of up to 75 percent over traditional solutions.

The AD9959 and AD9958 are optimized for applications that require complex high speed synthesis up to 200 MHz, including phased-array radar/sonar systems, automatic test equipment, medical imaging and optical communications systems.

Precise Synchronization, Low Power

In order to alleviate the design complexities typically involved in the synchronization of multiple DDS devices, the independent channels of the AD9959 and AD9958 are internally synchronized by a common reference clock. Programmable channel control allows for correction of imbalances in external signal paths due to analog processing, such as filtering, amplification, or PCB layout mismatches. If additional channels are required, the AD9959 and AD9958 allow daisy chaining of additional DDS chips. The devices also offer extremely low power consumption of less than 165 mW per channel.

Independent Channel Phase, Frequency, and Amplitude Control

Each channel of the four-channel AD9959 and the two-channel AD9958 incorporates a high speed 10-bit DAC with excellent wideband and narrowband SFDR (spurious free dynamic range). Each fully independent programmable channel provides 14-bits of phase offset tuning, 32-bit frequency resolution and 10-bit amplitude control. The device also supports direct or linear sweep modulation, while achieving channel isolation of greater than 60 dB. The integrated 32-bit frequency tuning word enables each channel to be programmed to resolutions of 116 mHz or less with a sampling clock of up to 500 MSPS.

Part#	Master fclk	Resolution (Bits)	Max Output Freq	Power Dissipated (max)	On-Board LPF	I & Q Output
AD9854	300MHz	12	120MHz	3W	Yes (120MHz)	Single Channel Differential
AD9954	400MHz	14	150MHz	250mW (TBC)	Yes (TBC)	Single Channel Differential
AD9959	500MHz	10	200MHz	680mW	Yes (200MHz)	4 Channels Differential and/or Single ended
AD9858	1000MHz	10	400MHz	2.5W	Yes (200MHz and 300MHz)	Single Channel Differential

Table 2. DDS comparison.

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